VINAYAKA MISSIONS UNIVERSITY, SALEM

TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E- EMBEDDED SYSTEM TECHNOLOGY

FULL TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2015 REGULATION

I SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Applied Mathematics for Electronics Engineers (common to AE, EST, VLSI)	MATHS	3	1	0	4
2	Advanced Digital System Design (common to AE, EST, VLSI)	ECE	3	0	0	3
3	Real Time Operating Systems	ECE	3	0	0	3
4	Design of Embedded Systems	ECE	3	1	0	4
5	Data Communication & Networks	ECE	3	0	0	3
6	Elective I	ECE	3	0	0	3
PRACTICAL						
7	Embedded Systems Lab I	ECE	0	0	2	2
TOTAL						22

II SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Computer Architecture & Parallel Processing (common to AE, EST, VLSI)	CSE	3	0	0	3
2	Software Technology for Embedded Systems	ECE	3	1	0	4
3	VLSI Architecture and Design methodologies	ECE	3	1	0	4
4	Advanced Digital Image Processing	ECE	3	1	0	4
5	Elective II	ECE	3	0	0	3
6	Elective III	ECE	3	0	0	3
PRACTICAL						
7	Embedded Systems Lab II	ECE	0	0	0	2
TOTAL						23

III SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Elective IV	ECE	3	0	0	3
2	Elective V	ECE	3	0	0	3
3	Elective VI	ECE	3	0	0	3
PRACTICAL						
4	Project Work Phase-I & Viva Voce	ECE	0	0	6	6
TOTAL						15

IV SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
PRACTICAL						
1	Project Work Phase-II & Viva Voce	ECE	0	0	12	12
TOTAL						12

Overall Credits

S.No	Semester	Credits
1	I	22
2	II	23
3	III	15
4	IV	12
Total		72

ELECTIVES LIST

S.No.	Course Title	Offering Department	L	T	P	C
1	ASIC Design	ECE	3	0	0	3
2	Multiprocessor	ECE	3	0	0	3
3	Wireless Security	ECE	3	0	0	3
4	Evolutionary Computing	ECE	3	0	0	3
5	Medical Image Processing	ECE	3	0	0	3
6	3 Dimensional Network on Chip	ECE	3	0	0	3
7	Advanced Robotics & Automation	ECE	3	0	0	3
8	System on Chip	ECE	3	0	0	3
9	Pattern Recognition & Artificial Intelligent Techniques	ECE	3	0	0	3
10	Wavelets & Multi-resolution Processing	ECE	3	0	0	3
11	Neural Computing	ECE	3	0	0	3
12	Advanced Wireless Networks	ECE	3	0	0	3
13	Automotive Electronics	ECE	3	0	0	3
14	Internetworking Multimedia	ECE	3	0	0	3
15	DSP Processors	CSE	3	0	0	3
16	Real Time Systems	ECE	3	0	0	3
17	VLSI Signal Processing	ECE	3	0	0	3
18	Low Power VLSI Design	ECE	3	0	0	3
19	Mobile Computing	ECE	3	0	0	3
20	Digital Control Systems	EEE	3	0	0	3

	SEMESTER I	L	T	P	C
	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS (common to AE, EST, VLSI)	**3**	**1**	**0**	**4**

AIM:

Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:

- To understand the concepts of fuzzy logic.
- To make the student learn different matrix methods and some of the applications.
- To understand the concepts of random variables.
- To make the student learn dynamic programming and their applications.
- To understand the concepts of different queuing models.

UNIT I: FUZZY LOGIC **9**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY **9**

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES **9**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING **9**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V: QUEUEING MODELS **9**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7^{th} Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7^{th} edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2^{nd} edition, John Wiley and Sons, New York (1985).

	SEMESTER I	L	T	P	C
	ADVANCED DIGITAL SYSTEM DESIGN (common to AE, EST, VLSI)	**3**	**0**	**0**	**3**

AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA 9

Shannon's expansion theorem, Conseusus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC 9

Linear seperability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS 9

Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS 9

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES 9

Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS

REFERENCES:

1. William I. Fletcher, “An Engineering Approach to Digital Design" , Prentice Hall of India, 1996.
2. James E. Palmer, David E. Perlman, “Introduction to Digital Systems", Tata McGraw Hill, 1996.
3. N.N. Biswas, "Logic Design Theory", Prentice Hall of India, 1993.
4. S. Devadas, A. Ghosh and K. Keutzer, "Logic Synthesis", Mc Graw Hill, 1994.

	Semester I	L	T	P	C
	REAL TIME OPERATING SYSTEMS	**3**	**0**	**0**	**3**

AIM:

The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:

To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS 9

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes –Introduction to Distributed operating system – Distributed scheduling.

UNIT II: OVERVIEW OF RTOS 9

RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT I II: REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT I V: REAL TIME KERNEL 9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V: RTOS APPLICATION DOMAINS 9

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

TOTAL: 45 HOURS

REFERENCES:

1. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.
2. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.

3 Charles Crowley, “Operating Systems-A Design Oriented approach” McGraw Hill 1997.

4 C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.

5. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 1999.

6. Mukesh Sighal and N G Shi “Advanced Concepts in Operating System”, McGraw Hill 2000.

	Semester I	L	T	P	C
	DESIGN OF EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

AIM:

This course aims to give the knowledge for students on all aspects of the design and development of an embedded system, including hardware and embedded software development.

OBJECTIVE:

At the end of this course the student can utilizes and applies the skills and knowledge upon embedded hardware as well as software development.

UNIT I: EMBEDDED DESIGN LIFE CYCLE **9**

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.

UNIT II: PARTITIONING DECISION **9**

Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory mapped access – speed and code density

UNIT III: INTERRUPT SERVICE ROUTINES **9**

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyser – Caches – Computer optimisation – Statistical profiling

UNIT IV: IN CIRCUIT EMULATORS **9**

Buller proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

UNIT V: TESTING **9**

Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. Arnold S. Berger – “Embedded System Design”, CMP books, USA 2002.
2. Sriram V. Iyer, Pankaj Gupta, “Embedded Real-time Systems. Programming”, Tata McGraw Hill, 2004.
3. ARKIN, R.C., Behaviour-based Robotics, The MIT Press, 1998.

	Semester I	L	T	P	C
	DATA COMMUNICATION AND NETWORKS	**3**	**0**	**0**	**3**

AIM:

To introduce concepts of data communication networks.

OBJECTIVE:

To make the student learn, all parts of communication software in layered architecture.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS **9**

An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS **9**

Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER **9**

Datagram and virtual circuit service - Routing principles - Internet protocols IPVI Addressing and routing datagram format _ IP fragmentation and reassembly - ICMP routing in the internet - Router - Input ports - Switching fabrics - Output ports - Queuing - IPV6 packet format transition from IPV4 to IPV6 Multicast routing.

UNIT IV DATA LINK AND MAC LAYER **9**

Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM- X.2.5 and Frame relay.

UNIT V NETWORK SECURITY AND MULTIMEDIA 9

Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL: 45 HOURS

REFERENCES

1. K.Kurose and K.W.Ross - "Computer network" Addison Wesley.(1997)
2. A.S . Tanenbaum "Computer Networks "- (3/e), (2001).
3. T.N.Saadavi,M.H.Ammar & AL . Halleem" Fundamentals of Telecommunication Networks " -
4. Wiley J.K.Buford - "Multimedia Systems" - Addison Wesley.(2001)

	Semester I	L	T	P	C
	EMBEDDED SYSTEMS LAB I	**0**	**0**	**2**	**2**

LIST OF EXPERIMENTS

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers
   i) I/O Programming, Timers, Interrupts, Serial port programming
   ii) PWM Generation, Motor Control, ADC/DAC, LCD and RTC Interfacing, Sensor Interfacing
   iii) Both Assembly and C programming
2. Design with 16 bit processors
   I/O programming, Timers, Interrupts, Serial Communication,
3. Design with ARM Processors.
   I/O programming, ADC/DAC, Timers, Interrupts,
4. Study of one type of Real Time Operating Systems (RTOS)
5. Electronic Circuit Design of sequential, combinational digital circuits using CAD Tools
6. Simulation of digital controllers using MATLAB/LabVIEW.
7. Programming with DSP processors for
   Correlation, Convolution, Arithmetic adder, Multiplier, Design of Filters - FIR based , IIR based
8. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD
   Design and Implementation of simple Combinational/Sequential Circuits
9. Network Simulators
   Simple wired/ wireless network simulation using NS2
10. Programming of TCP/IP protocol stack.

TOTAL: 30 HOURS

REFERENCES:

1. Mohamammad Ali Mazidi & Mazidi ‘ 8051 Microcontroller and Embedded Systems’, Pearson Education
2. Mohammad Ali Mazidi, Rolind Mckinley and Danny Causey, ‘PIC Microcontroller and Embedded Systems’ Pearson Education
3. Jan Axelson ‘Embedded Ethernet and Internet Complete’, Penram publications
4. Kraig Mitzner, ‘Complete PCB Design using ORCAD Capture and Layout’, Elsevier
5. Woon-Seng Gan, Sen M. Kuo, ‘Embedded Signal Processing with the Micro Signal Architecture’, John Wiley & Sons, Inc., Hoboken, New Jersey 2007
6. U. Meyer-Baese ‘Digital Signal Processing using Field Programmable Gate Arrays’, Springer
7. Dogan Ibrahim, ‘Advanced PIC microcontroller projects in C’, Elsevier 2008

	Semester II	L	T	P	C
	COMPUTER ARCHITECTURE & PARALLEL PROCESSING (common to AE, EST, VLSI)	**3**	**0**	**0**	**3**

AIM:

Any Embedded design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:

- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING 9

Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.

Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLGIES 9

Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING 9

Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES 9

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V-SOFTWARE & PARALLEL PROCESSING 9

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:

1. Kai Hwang "Advanced Computer Architecture", Tata McGraw Hill International, 2001.

REFERENCE BOOKS:

1.John L. Hennessy, David A. Petterson, "Computer Architecture: A Quantitative Approach", 4th Edition, Elsevier, 2007.

2.Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced computer Architecture – A design Space Approach". Pearson Education,2003.

3.David E. Culler, Jaswinder Pal Singh with Anoop Gupta “Parallel Computer Architecture” ,Elsevier, 2004.
4.John P. Shen. “Modern processor design Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
5.Sajjan G. Shiva “Advanced Computer Architecture”, Taylor & Francis, 2008.
6.V.Rajaraman, C.Siva Ram Murthy, “Parallel Computers- Architecture and Programming”, Prentice Hall India, 2008.

	Semester II	L	T	P	C
	SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

AIM:

To introduce some C concepts relavant to embedded systems with 80x86 family as basis and UML.

OBJECTIVE:

To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

UNIT I LOW LEVEL PROGRAMMING IN C 9

Primitive data types – Functions – recursive functions – Pointers - Structures – Unions – Dynamic memory allocations – File handling – Linked lists

UNIT II C AND ASSEMBLY 9

Programming in Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

UNIT III OBJECT-ORIENTED ANALYSIS AND DESIGN 9

Connecting the Object Model with the Use Case Model. Key Strategies for Object-Identification - Underline the Noun Strategy. Identify the Casual Objects - Identify Services (Passive Contributors) - Identify Real-World Items - Identify Physical Devices - Identify Key Concepts - Identify Transactions - Identify Persistent Information - Identify Visual Elements. Identify Control Elements - Apply Scenarios.

UNIT IV UNIFIED MODELLING LANGUAGE 9

Object State Behaviour - UML State charts - Role of Scenarios in the Definition of Behaviour - Timing Diagrams - Sequence Diagrams - Event Hierarchies - Types and Strategies of Operations - Architectural Design in UML Concurrency Design - Representing Tasks - System Task Diagram - Concurrent State Diagrams - Threads. Mechanistic Design - Simple Patterns.

UNIT V CASE STUDIES 9

Multi threaded applications – assembling embedded applications – polled waiting loop and interrupt driven I/O – preemptive kernels and shared resources - system timer – scheduling – client server computing.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. Bruce Powel Douglas, “Real-Time UML, Second Edition: Developing Efficient Objects for Embedded Systems (The Addison-Wesley Object Technology Series)”, 2 edition (October 29, 1999), Addison-Wesley.
2. Hassan Gomma, “Designing Concurrent, Distributed, and Real-Time applications with UML.
3. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet” PHI 2002.

	Semester II	L	T	P	C
	VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	**3**	**1**	**0**	**4**

AIM:

This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:

- At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

UNIT I INTRODUCTION 9

Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon's expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

UNIT II ANALOG VLSI AND HIGH SPEED VLSI 9

Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

UNIT III PROGRAMMABLE ASICS 9

Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

UNIT IV PROGRAMMABLE ASIC DESIGN SOFTWARE 9

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 - Altera MAX 9000 - Design systems – Logic synthesis – Half gate ASIC – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation

UNIT V LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

1. William I. Fletcher “An Engineering approach to Digital Design” Prentice Hall of India 1996

2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986

3. M.J.S Smith “Application – specific integrates circuits”, Addison Wesley Longman Inc.1997

4. Frederick J. Hill and Gerald R. Peterson, “Computer Aided Logical Design with emphasisonVLSI”.

	Semester II	L	T	P	C
	ADVANCED DIGITAL IMAGE PROCESSING	**3**	**1**	**0**	**4**

AIM:

This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGETRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION 9

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION 9

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding, Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression

UNIT IV: COLOUR IMAGE PROCESSING **9**

Introduction, Light and colour, colour formation, Human perception of colour, colour model The chromaticity diagram, colour image quatization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING **9**

Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation,Basic Morphological Algorithms,Extension to Gray scale Images.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1) S.Jayaraman, S.Esakkirajan and T.VeeraKumar, "Digital Image processing, Tata Mc Graw Hill publishers, 2009

2) Gonzalez, R.E.Woods, "Digital Image Processing", 3rd Edition, Pearson Education, India, 2009.

3) John W.Woods, "Multidimensional Signal, Image and Video Processing and Coding" Elsevier Academic Press Publications 2006, ISBN-13: 978-0-12– 088516-9.

	Semester II	L	T	P	C
	EMBEDDED SYSTEMS LAB – II	**0**	**0**	**2**	**2**

1. ATMEL CPLDs – Prochip designer

a) Schematic entry

b) VHDL entry

2. AT40K FPGA series – synthesis – design – simulation of application programs

3. Xilinx EDA design tools – device programming –PROM programming

4. ALTERA and Mentor graphics – IC design tools

5. Code compressor studio for embedded DSP using Texas tool kit

6. Cell based ASICs – sample programs for risk and security plans

7. IPCORE usage in VOIP through SoC2 tools

8. FPSLIC synthesis testing and examples

9. Third party tools for embedded java and embedded C++ applications through cadence tools.

TOTAL: 30 HOURS

	ELECTIVE	L	T	P	C
	ASIC DESIGN	**3**	**0**	**0**	**3**

AIM:

As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:

To make the student learn the fundamentals of ASIC and its design methods.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS

REFERENCES:

1. M.J.S .Smith, “Application - Specific Integrated Circuits “- Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	MULTIPROCESSOR	**3**	**0**	**0**	**3**

AIM:

To understand performance metrics and be able to analyze scalability and speedup factors of multiprocessor systems.

OBJECTIVE:

- To Learn parallel computer architectures with multiprocessor and multi-core.
- To understand Master parallel programming techniques.
- To gain experiences of applying parallel programming to achieve performance gains from multiprocessor and multi-core computer systems.

Unit I

Application-Specific Multiprocessors **9 Hours**

Parallel architecture classifications - Exploiting instruction-level parallelism - Dataflow DSP architectures - Systolic and wavefront arrays - Multiprocessor DSP architectures - Single-chip multiprocessors , Terminology: Graph data structures - Dataflow graphs - Computation graphs - Petri Nets - Synchronous dataflow – SDF and Expansion graphs - Synchronous languages - HSDFG concepts and notations - Complexity of algorithms - Maximum cycle mean.

Unit II

Dataflow and Scheduling Models **9 Hours**

Dataflow Models: Scalable synchronous, Cyclostatic, Multidimensional synchronous, Parameterized dataflow models – Reactive process networks - Integrating dataflow and state machinemodels - Controlled dataflow actors , Scheduling Models: Task-level parallelism and data parallelism, Static versus dynamic scheduling strategies, Fully static, Self-timed, Dynamic, Quasi-static, schedules, Scheduling Algorithms : Stone's assignment algorithm, List scheduling algorithms, Clustering algorithms, Integrated scheduling algorithms, Pipelined scheduling.

Unit III

Ordered-Transactions Strategy **9 Hours**

Shared bus architecture – Inter-processor communication mechanisms - Design of an ordered memory access multiprocessor - Design details of a prototype - Hardware and software implementation - Ordered I/O and parameter control – Inter-processor communication graph (Gipc) - Execution time estimates - Ordering constraints viewed as added edges - Periodicity - Optimal order - Effects of changes in execution times - Effects of inter-processor communication costs - Application examples.

Unit IV

Synchronization **9 Hours**

The barrier MIMD technique - Redundant synchronization removal in non-iterative dataflow - Analysis of self-timed execution - Strongly connected components and buffer size bounds - Synchronization model - A synchronization cost metric – Removing redundant synchronizations - Insertion of delays – Definition, properties of resynchronization - Relationship to set covering - Intractability of resynchronization - Heuristic solutions - Chainable synchronization graphs - Resynchronization of constraint graphs for relative scheduling - Elimination of synchronization edges – LCR - Intractability of LCR - Two-processor systems - A heuristic for general synchronization graphs - Integrated Synchronization Optimization

Unit V

Run Time System **9 Hours**

Exceptions, Interrupts, and Traps - Application Binary Interface Considerations - Loading Programs - Data Layout – Accessing Global Data - Calling Conventions - Advanced ABI Topics - Code Compression - Multiprocessing and Multithreading.

Total: 45 Hours

REFERENCES:

1. SunderrajanSriram and Shuvra S Battacharya, *Embedded Multiprocessos Scheduling and Synchronization*, Marcel Dekker Incorporated, 2002.

2. Joseph A Fisher, Polo Faraboschi, CliffYoung, *Embedded Computing: A VLIW Approach to Architecture,*Elseiver Publications, 2008

3. Maurice Herlihy, NirShavit, *The Art of Multiprocessor Programming,* Morgan Kaufmann, 1st edition, 2008.

	ELECTIVE	L	T	P	C
	WIRELESS SECURITY	**3**	**0**	**0**	**3**

AIM:

To understand the security principles of wireless networks.

OBJECTIVE:

- To explore variety of attacks and threats and its impact on MAC layer and Network layer
- To study characteristics, vulnerabilities and challenges of ad hoc networks
- To provide solution for covering the security principles and flaws of popular wireless technologies
- To evaluate the performance of secured routing protocols in MANETs.

Unit I – Attacks on Routing Protocols **9 Hours**

Vulnerability of MANET to attack - review of AODV and DSR - type of attack - active and passive - internal and external - behavior of malicious node - black hole, DoS, Routing table overflow, Impersonation, Energy consumption, Information Disclosure - Misuse type – Misuse goals – Security flaw in AODV -attack on AODV - wormhole and rushing attack -Performance analysis of AODV in the presence of malicious node.

Unit II – Intrusion Detection in Wireless Ad Hoc Networks **9 Hours**

Problem in current IDS techniques - requirements of IDS - classification of IDS – Network and host based - anamoly detection, misuse detection, specification based - intrusion detection in MANETs using distributed IDS and mobile agents - AODV protocol based IDS - Intrusion resistant routing algorithms – Comparison of IDS.

Unit III – Mitigating Techniques for Routing Misbehavior **9 Hours**

Watchdog, Parthrater, Packet leashes and RAP.

Unit IV – Secure Routing Protocols: **9 Hours**

Self organized network layer security in MANETs - mechanism to improve authentication and integrity in AODV using hash chain and digital signatures - on demand secure routing protocol resilent to Byzantine failures - ARIADNE, SEAD, SAR, and ARAN.

Unit V – Challenges in Routing Security **9 Hours**

Security - Challenges and solutions - Providing Robust and Ubiquitous security support - Adaptive security for multilevel Ad Hoc Network - Denial of service Attack at the MAC layer - Detection and handling of MAC layer Misbehavior.

REFERENCES:

1. C.Siva Ram Murthy and B.S.Manoj, *AdHoc Wireless Networks: Architectures and Protocols*, Prentice Hall PTR, 2004.
2. Ivan Stojmenović, *Handbook of Wireless Networks and Mobile Computing*, Wiley, 2002.
3. Hongmei Deng, Wei Li and Dharma P. Agrawal, *Routing Security in Wireless Ad Hoc Networks*, IEEE Communication Magazine, Oct 2002.
4. Peng Ning, Kun Sun, *How To Misuse AODV: A Case Study of Insider Attacks Again Mobile Ad Hoc Routing Protocols* in proceeding of the 4th annaul IEEE information assurance workshop, page 60 – 67 west point, June 2003.
5. Amitabh Mishra, *Intrusion Detection in Wireless Ad Hoc Networks*, IEEE Wireless Communication, February 2004.
6. S.Marti, *Mitigating Routing Misbehaviour in Mobile Ad Hoc Networks*, ACM MOBICOM, 2000.

	ELECTIVE	L	T	P	C
	EVOLUTIONARY COMPUTING	**3**	**0**	**0**	**3**

AIM:

The students can able to analyze the procedure for various principles of Evolutionary computing in real world problem.

OBJECTIVE:

- To study different types of optimization techniques.
- To understand the concepts of genetic algorithms.
- To attain sound knowledge applications of soft computing.

Unit I – Fuzzy Systems **9 Hours**

Fuzzy set theory-fuzzy rules and fuzzy reasoning-fuzzy inference systems-decomposition-fuzzy automata and languages-fuzzy control methods.

Unit II – Neural Networks **9 Hours**

Basic concepts-knowledge based processing-single layer perceptron-multilayer perceptron-supervised and unsupervised learning-feed forward and back propagation and counter propagation networks-kohens self organizing networks-Hopfield networks.

Unit III – Neuro Fuzzy Modeling **9 Hours**

Adaptive neuro fuzzy inference systems-classification and regression trees- data clustering-rule base structure identification-neuro fuzzy controls.

Unit IV – Genetic Algorithms **9 Hours**

Basics of GA- choice of encoding-selection probability-mutation and crossover-fitness evaluation improving convergence rate-a simplex GA- Hybrid approach.

Unit V – Applications of Soft Computing **9 Hours**

Fuzzy techniques for inverted pendulum case-SIRM fuzzy systems-MCDM for weather forecasting and financial marketing-Neural networks for pattern recognition-TS problems-Routers - GA application to metabolic modeling.

REFERENCES:

1. Jang J.S.R.,Sun C.T and Mizutani E,"*Neuro Fuzzy and Soft computing",* Pearson Education (Singapore), 2006
2. David E.Goldberg, **"***Genetic Algorithms in Search, Optimization, and Machine Learning",* Pearson Education, Asia, 2001**.**
3. Timothy J.Ross**, "***Fuzzy Logic Engineering Applications",* McGrawHill, NewYork, 2002.
4. S.Rajasekaran and G.A.Vijayalakshmi Pai, **"***Neural networks, Fuzzy logics and Genetic algorithms"***,** Prentice Hall of India, 2003.
5. George J.Klir and Bo Yuan,"*Fuzzy Sets and Fuzzy Logic***",** Prentice Hall Inc., New Jersey, 2002.

	ELECTIVE	L	T	P	C
	MEDICAL IMAGE PROCESSING	**3**	**0**	**0**	**3**

AIM:

To describe and determine the performance of different Image reconstruction techniques.

OBJECTIVE:

- To study about various medical image acquisition methods.
- To understand 2D and 3D image reconstruction techniques.
- To gain sound knowledge about CT, MRI, nuclear and ultrasound imaging.
- To realize the factors those affect the quality of medical images.

Unit I – Acquisition of Images **9 Hours**

Introduction to Imaging Techniques- Single crystal scintillation camera – Principles of scintillation camera – multiple crystal scintillation camera –solid state camera –rectilinear scanner –Emission computed Tomography.

Unit II – Mathematical Preliminaries for Image Reconstruction **9 Hours**

Image Reconstruction from Projections in Two dimensions –Mathematical Preliminaries for Two and Three dimensional Image Reconstructions –Radon Transform –Projection Theorem –central slice Theorem – Sinogram – Two Dimensional Projection Reconstruction –Three Dimensional Projection Reconstruction – Iterative Reconstruction Techniques.

Unit III – Fluoroscopy, CT, Image quality **9 Hours**

Digital fluoroscopy – Automatic Brightness control- cinefluorography –Principles of computed Tomographic Imaging- Reconstruction algorithms- Scan motions – X –ray sources ***Influences of Images quality:*** Unsharpness – contrast- Image Noise.

Unit IV – Magnetic Resonance Imaging and Spectroscopy **9 Hours**

Fundamentals of magnetic resonance – overview – Pulse techniques – spatial encoding of magnetic resonance imaging signal – motion suppression techniques – contrast agents- tissue contrast in MRI – MR angiography, spectrography.

Unit V – Ultra sound, Neuro magnetic Imaging **9 Hours**

ultra Sound: Presentation modes – Time required to obtain Images – System components, signal processing – dynamic Range – Ultrasound Image Artifacts – Quality control, Origin of Doppler shift – Limitations of Doppler systems. ***Neuromagnetic Imaging:*** Background

REFERENCES:

1. William R. Hendee, E. Russell Ritenour, *Medical Imaging Physics:* A John Wiley & sons, Inc., Publication, Fourth Edition 2002.
2. Z.H. Cho., J-oie, P. Jones and Manbir Singh, *Foundations of Medical Imaging:* John Wiley and sons Inc.
3. Avinash C. Kak, Malcolm Shaney, *Principles of Computerized Tomographic Imaging*, IEEE Press, Newyork-1998.

	ELECTIVE	L	T	P	C
	3 DIMENSIONAL NETWORK ON CHIP	**3**	**0**	**0**	**3**

AIM:

The students can able to learn advanced technologies in the fields of NOC along with the fundamental concepts.

OBJECTIVE:

- To understand the fundamentals of 3D NOC.
- To impart knowledge about testing and energy issues in NOC.
- To understand the router architectures in 3D NOC.

Unit I

Introduction to Three Dimensional NOC **9 Hours**

Three - Dimensional Networks-on-Chips Architectures. – Resource Allocation for QoS On-Chip Communication – Networks-on-Chip Protocols - On-Chip Processor - Traffic Modeling for Networks-on-Chip.

Unit II

Test and Fault Tolerance of NOC **9 Hours**

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures- Monitoring Services for Networks-on-Chips.

Unit III

Energy and Power Issues of NOC **9 Hours**

Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips.

Unit IV

Micro-Architecture of NOC Router **9 Hours**

Baseline NoC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers RoCo: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks-on-Chip Architectures.

Unit V

DimDE Router for 3D NOC **9 Hours**

A Novel Dimensionally Decomposed Router for On-Chip Communication in 3D Architectures - Digest of Additional NoC MACROArchitectural Research.

Total: 45 Hours

REFERENCES:

1. ChrysostomosNicopoulos,VijaykrishnanNarayanan,ChitaR.Das,*Networks-on- Chip Architectures A Holistic Design Exploration,* Springer,2009.

2. Fayezgebali,Haythamelmiligi,HqhahedWatheqE1-Kharashi, *Networks-on-Chips theory and practice,* CRC press, 2009.

3. Axel Jantsch , Hannu Tenhunen, *Networks on Chip,* Publisher: Springer; Soft cover reprint of hardcover 1st ed. 2003 edition (November 5, 2010).

4. Giovanni De Micheli , Luca Benini, *Networks on Chips: Technology and Tools (Systems on Silicon)*, Publisher: Morgan Kaufmann; 1 edition (August 3, 2006).

5. Jose Flich , Davide Bertozzi, *Designing Network On-Chip Architecturesin the Nanoscale Era,* (Chapman & Hall/CRC Computational Science), Publisher: Chapman and Hall/CRC; 1 edition (December 18,2010).

	ELECTIVE	L	T	P	C
	ADVANCED ROBOTICS & AUTOMATION	**3**	**0**	**0**	**3**

AIM:

The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:

At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION **9**

Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS **9**

Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS **9**

Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion.

UNIT IV ROBOT APPLICATONS **9**

Material Transfer & Machine Loading / Unloading General Consideration in robot material handling transfer applications – Machine loading and unloading. Processing Operations Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

UNIT V ASSEMBLY AND INSPECTION **9**

Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

TOTAL: 45 HOURS

REFERENCES:

1. Fu, Gonazlez.K.S., R.C. and Lee, C.S.G., Robotics (Control, Sensing, Vision and Intelligence), McGraw Hill, 1968
2. Wesley.E, Snyder.R, Industrial Robots, "Computer Interfacing and Control", Prentice Hall International Edition, 1988
3. Asada and Slotine, "Robot analysis and Control", John Wiley and sons, 1986
4. Philippe Coiffet, "Robot technology" - Vol.II (Modelling and Control), Prentice Hall Inc., 1983
5. Groover.M.P., Mitchell, Weiss, "Industrial Robotics Technology Programming and Applications", Tata McGraw Hill, 1986

	ELECTIVE	L	T	P	C
	SYSTEM ON CHIP	**3**	**0**	**0**	**3**

AIM:

The students can able to gain knowledge about SoC Design Methodology.

OBJECTIVE:

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Unit I

Introduction **9 Hours**

System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC design issues -SoC challenges and components.

Unit II **9 Hours**

Design Methodological For Logic Cores

SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores –Designing with hard cores, soft cores- Core and SoC design examples.

Unit III **9 Hours**

Design Methodology for Memory and Analog Cores

Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase- located loops –High I/O.

Unit IV **9 Hours**

Design Validation

Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification. Case Study: Validation and test of systems on chip

Unit V **9 Hours**

Soc Testing

SoC Test Issues – Testing of digital logic cores –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self method –testing of embedded memories.

Total: 45 Hours

REFERENCES:

1. Rochit Rajsunah, *System-on-a-chip: Design and Test*, Artech House, 2007.
2. Prakash Raslinkar, Peter Paterson & Leena Singh, *System-on-a-chip verification: Methodology and Techniques*, Kluwer Academic Publishers, 2000.
3. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, *Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems*, Springer, 2007.
4. L.Balado, E. Lupon, *Validation and test of systems on chip*, IEEE conference on ASIC/SOC,1999.
5. A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, *Integrating BIST techniques for on-line SoC testing*, IEEE Symposium on On-Line testing, 2005.

	ELECTIVE	L	T	P	C
	PATTERN RECOGNITION & ARTIFICIAL INTELLIGENT TECHNIQUES	**3**	**0**	**0**	**3**

AIM:

To gain the knowledge about the procedure for various pattern recognition principles in real world problem.

OBJECTIVE:

- To understand different supervised and unsupervised learning techniques.
- To obtain sound knowledge on recent advancement on pattern recognition techniques.

Unit I – Pattern Classifier **9 Hours**

Overview of pattern recognition - Discriminant functions - Supervised learning - Parametric estimation - Maximum likelihood estimation - Bayesian parameter estimation - Perceptron algorithm - LMSE algorithm - Problems with Bayes approach - Pattern classification by distance functions - Minimum distance pattern classifier.

Unit II – Unsupervised Classification **9 Hours**

Clustering for unsupervised learning and classification - Clustering concept - C-means algorithm – Hierarchical clustering procedures - Graph theoretic approach to pattern clustering - Validity of clustering solutions.

Unit III – Structural Pattern Recognition **9 Hours**

Elements of formal grammars - String generation as pattern description - Recognition of syntactic description - Parsing - Stochastic grammars and applications - Graph based structural representation.

Unit IV – Feature Extraction and Selection **9 Hours**

Entropy minimization - Karhunen - Loeve transformation - Feature selection through functions approximation -Binary feature selection.

Unit V – Recent Advances **9 Hours**

Neural network structures for Pattern Recognition - Neural network based Pattern associators – Unsupervised learning in neural Pattern Recognition - Self organizing networks - Fuzzy logic – Fuzzy pattern classifiers - Pattern classification using Genetic Algorithms.

REFERENCES:

1. 1.Robert J.Schalkoff, *Pattern Recognition: Statistical, Structural and Neural Approaches*, John Wiley &Sons Inc., New York, 2007.
2. Tou and Gonzales, *Pattern Recognition Principles*, Wesley Publication Company, London, 1974.
3. Duda R.O., Hart.P.E., and Strok, *Pattern Classification*, second Edition Wiley, New York, 2008.
4. 4.Morton Nadier and Eric Smith P., *Pattern Recognition Engineering*, John Wiley & Sons, New York, 1993.
5. IEEE Transaction on Pattern Recognition Techniques 2006.
6. IEEE Engineering Medicine and Biology Magazine 2006.

	ELECTIVE	L	T	P	C
	WAVELETS & MULTI-RESOLUTION PROCESSING	**3**	**0**	**0**	**3**

AIM:

To gain the knowledge and skills about various image processing applications.

OBJECTIVE:

- To study the fundamentals of vector and signal spaces.
- To explore the concepts of multi resolution analysis of signals.

Unit I – Introduction **9 Hours**

Vector Spaces - properties - dot product - basis - dimension, orthogonality and orthonormality - relationship between vectors and signals - Signal spaces - concept of Convergence - Hilbert spaces for energy signals - Generalized Fourier Expansion.

Unit II – Multi Resolution Analysis **9 Hours**

Definition of Multi Resolution Analysis (MRA) – Haar basis - Construction of general orthonormal MRAWavelet basis for MRA – Continuous time MRA interpretation for the DTWT – Discrete time MRABasis functions for the DTWT – PRQMF filter banks.

Unit III – Continuous Wavelet Transform **9 Hours**

Wavelet Transform - definition and properties - concept of scale and its relation with frequency - Continuous Wavelet Transform (CWT) - Scaling function and wavelet functions (Daubechies, Coiflet, Mexican Hat, Sinc, Gaussian, Bi-Orthogonal) - Tiling of time -scale plane for CWT.

Unit IV – Discrete Wavelet Transform **9 Hours**

Filter Bank and sub band coding principles - Wavelet Filters - Inverse DWT computation by Filter banks - Basic Properties of Filter coefficients - Choice of wavelet function coefficients - Derivations of Daubechies Wavelets -Mallat's algorithm for DWT – Multi-band Wavelet transforms. Lifting Scheme: Wavelet Transform using Poly phase matrix Factorization - Geometrical foundations of lifting scheme - Lifting scheme in Z – domain.

Unit V – Applications **9 Hours**

Signal Compression – Image Compression techniques: EZW-SPHIT Coding Image denoising techniques-Noise estimation - Shrinkage rules - Shrinkage Functions - Edge detection and object Isolation, Image Fusion, and Object Detection. Curve and Surface Editing-Variation modeling and finite element method using wavelets.

REFERENCES:

1. G,.Strang and T.Nguyen, *Wavelets and Filter Banks*, Wellesley Cambridge Press, 1996
2. M .Vetterli and J.Kovacevic, *Wavelets and Sub-band Coding*, Prentice Hall, 1995
3. S.Mallat., *Wavelet Tour of Signal Processing*, Academic Press, 2008.
4. www.multiresolution.com
5. www.wavelet.org
6. IEEE transactions on Image Processing.

	ELECTIVE	L	T	P	C
	NEURAL COMPUTING	**3**	**0**	**0**	**3**

AIM:

To apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with soft computing and networking problems that require advanced knowledge within the field.

OBJECTIVE:

- To study the concepts of biological and artificial neurons
- To explore the fundamentals of various algorithms related to supervised neural networks and its applications
- To explore the Applications of various algorithms related Genetic algorithms and SVM

Unit I – Fundamental Concepts and Models of Artificial Neural Systems 9 Hours

Biological Neurons and their Artificial models, Models of Artificial Neural Networks, Learning and Adaptation, Neural Network Learning Rules, Single Layer Perceptron Classifiers.

Unit II – *BPN and BAM* 9 Hours

Back Propagation Network, Generalised Delta Rule, BPN Application, Associative Memory Definition, BAM, Hop field Memory, Simulated Annealing-Boltzmann Machine.

Unit III – Other Networks 9 Hours

Counter Propagation Network, Feature Mapping, Self Organizing Feature Maps, Adaptive Resonance Theory (ART) Network-Spatio-temporal neural networks Descriptions and applications.

Unit IV – Genetic Algorithms & Implementation Techniques 9 Hours

The Appeal of Evolution, Search Spaces and Fitness Landscapes, Elements of Genetic Algorithms, Data Structures, Adaptive Encoding. Selective Methods, Genetic Operators, Fitness Scaling.

Unit V – Advances and Applications 9 Hours

Support Vector Machines, RBF Network, Neocognitron Evolving neural networks using GA, Applications of ANN in signal analysis and Medical image analysis.

REFERENCES:

1. Sathish Kumar, *Neural networks-A Class Room approach*, third edition, Tata Mc Graw Hill New Delhi, 2012
2. James Freeman A. and David Skapura M., *Neural Networks - Algorithms, Applications &Programming Techniques*, Addison Wesley, 1992.
3. Yegnanarayana B., *Artificial Neural Networks*, Prentice Hall of India Private Ltd., New Delhi, 1999.
4. Laurence Fausett, *Fundamentals of Neural Networks: Architecture, Algorithms and Applications*, Prentice Hall, 1994.
5. Simon Haykin, *"Neural Networks: A Comprehensive Foundation"*, 2nd Edition,Prentice HallIndia,2002..
6. David Goldberg, *Genetic Algorithms in Search, Optimization and Machine Learning*, Addison - Wesley USA, 1997.
7. Melanie Mitchell, *An Introduction to Genetic Algorithms*: Prentice Hall of India, New Delhi 1998.

	ELECTIVE	L	T	P	C
	ADVANCED WIRELESS NETWORKS	**3**	**0**	**0**	**3**

AIM:

To obtain awareness for adaptation in MAC, IP, protocols for advanced mobile networks.

OBJECTIVE:

- To study fundamentals of 4G networks
- To explore issues and challenges in designing adaptive MAC for adhoc networks
- To understand adaptation of the routing protocols in mobile networks
- To explore issues and challenges in sensor network deployment
- To develop security protocols for wireless networks

Unit I – Fundamentals of 4G Networks **9 Hours**

Protocol Boosters-Hybrid 4G Wireless Network Protocols-Green Wireless Networks-Physical Layer and Multiple Access-ATDMA-CDMA-OFDM.

Unit II – Adaptive MAC and Network Layer **9 Hours**

WLAN Enhanced Distributed Coordination Function- Adaptive MAC for WLAN – MAC for Wireless Sensor Networks-MAC for AdHoc Networks-Adaptive Network Layer- Graphs and Routing Protocols – Graph theory – Routing topology Aggregation – Network and Aggregation Models.

Unit III – Adaptive TCP Layer **9 Hours**

Introduction-TCP operations and Performance – TCP for Mobile Cellular Networks-RED Gateways for Congestion Avoidance- TCP for Mobile AdHoc Networks – Cross Layer optimization – Introduction to Mobility Management- Location Registration and Call Delivery in 4G.

Unit IV – AD HOC Networks **9 Hours**

Routing protocols – Hybrid Routing Protocols – Scalable Routing Strategies – Multipath Routing – Clustering Protocols – Caching Schemes for Routing- Distributed QoS Routing.

Unit V – Sensor Networks and Security **9 Hours**

Introduction – Sensor Networks parameters- Architecture – Mobile Sensor Networks Deployment- Directed Diffusion- Aggregation in Wireless Sensor Networks – Boundary Estimation – Back off Phenomenon- Data Funneling- Equivalent Transport Control Protocols in Sensor Networks – Security – Authentication – Security Architecture- Key management – Security management in GSM, UMTS – Security in AdHoc and Sensor Networks.

REFERENCES:

1. Young Kyun Kim and Ramjee Prasad,*4G Roadmap and Emerging Communication Technologies*, Universal Personal Communication Series, Artech House, Boston, 2006.
2. Hendrik Berndt, *Towards 4G Technologies*, Wiley Publishers, Lancaster, England, 2008.
3. IEEE Transactions on Networking.
4. IEEE Transactions on Mobile Computing.

	ELECTIVE	L	T	P	C
	AUTOMOTIVE ELECTRONICS	**3**	**0**	**0**	**3**

AIM:

To become knowledgeable about contemporary developments.

OBJECTIVE:

- To study the basics of automotive electronics.
- To understand sensors and activators.
- To study charging systems.

Unit I – Fundamentals of Automotive Electronics **9 Hours**

Current trends in automotive electronic engine management system, electromagnetic interference suppression, electromagnetic compatibility, electronic dashboard instruments, onboard diagnostic system. *Security and warning system.*

Unit II – Starting System **9 Hours**

Condition at starting, behavior of starter during starting, series motor and its characteristics, principle and construction of starter motor, working of different starter drive units, care and maintenances of starter motor. *Starter switches.*

Unit III – Charging System **9 Hours**

Generation of direct current, shunt generator characteristics, armature reaction, third brush regulation, cutout. Voltage and current regulators, compensated voltage regulator, alternators principle and constructional aspects. *Bridge rectifiers and new developments.*

Unit IV – Batteries and Accessories **9 Hours**

Principle and construction of lead acid battery, characteristics of battery, rating capacity and efficiency of batteries, various tests on batteries, maintenance and charging. Lighting system: insulated and earth return system, details of head light and side light, LED lighting system, head light dazzling and preventive methods. *Horn, wiper system and trafficator.*

Unit V – Sensors and Activators **9 Hours**

Types of sensors: sensor for speed, throttle position, exhaust oxygen level, manifold pressure, crankshaft position, coolant temperature, exhaust temperature, air mass flow for engine application. Solenoids. *Stepper motors and relay*.

REFERENCES:

1. Bechhold,*Understanding Automotive Electronics*, SAE, 1998.
2. W.H.Crouse ,*Automobile Electrical Equipment*, McGraw-Hill, 1996.
3. A W Judge, *Modern Electrical Equipment of Automobiles*, Chapman & Hall, 1992.
4. P.L.Kholi, *Automotive Electrical Equipment*, Tata McGraw-Hill, 1995.
5. Robert Bosch *Automotive Hand Book*, SAE, 2000.
6. A.P.Young, L.Griffiths *Automotive Electrical Equipment*, ELBS & New Press, 1999.
7. William.B.Riddens, *Understanding Automotive Electronics*, Butter worth Heinemann Woburn, 1998.

	ELECTIVE	L	T	P	C
	INTERNETWORKING MULTIMEDIA	**3**	**0**	**0**	**3**

AIM:

Main aim of this course is to make the students understand in identifying and analyzing the requirements that a distributed multimedia application may enforce on the communication network.

OBJECTIVE:

At the end of this course students have knowledge in distributing multimedia application over the communication network.

UNIT I MULTIMEDIA NETWORKING **9**

Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY **9**

Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL **9**

Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA - ON – DEMAND **9**

Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS **9**

MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TOTAL HOURS: 45

REFERENCES:

1. Jon Crowcroft, Mark Handley, Ian Wakeman. Internetworking Multimedia, Harcourt Asia Pvt.Ltd. Singapore, 1998.
2. B.O. Szuprowicz, Multimedia Networking, McGraw Hill, NewYork. 1995
3. Tay Vaughan, Multimedia making it to work, 4ed,Tata McGrawHill, NewDelhi,2000.

	ELECTIVE	L	T	P	C
	DSP PROCESSORS	**3**	**0**	**0**	**3**

AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP'S **9**

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSP's – Multiple access memory – Multi – port memory – VLIW architecture – pipelining – Special Addressing modes in P-DSP's – On Chip Peripherals.

UNIT II: TMS320C5X PROCESSOR **9**

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR **9**

Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

UNIT IV: ADSP PROCESSORS **9**

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS **9**

Architecture of TMS320C54X: Pipe line operation, Code Composer Studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45 HOURS

TEXT BOOK:

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" - Tata McGraw – Hill Publishing Company Limited. New Delhi, 2008.

REFERENCES:

1. User guides Texas Instrumentation, Analog Devices, Motorola.
2. Simon Haykin "Adaptive filter theory", Prentice Hall, 2001.
3. Anil K Jain "Fundamental of Digtal image processing", Prentice Hall, 1989.

	ELECTIVE	L	T	P	C
	REAL TIME SYSTEMS	**3**	**0**	**0**	**3**

AIM:

Since the concepts of real time systems and their analysis is very essential for embedded students this subject is given.

OBJECTIVE:

To make the student learn, all real time aspects of various system components, like OS, memory, communication and an introduction to reliability evaluation methods.

UNIT I INTRODUCTION 9

Introduction - issues in real time computing - structure of a real time system - task classes - performance measures for real time systems - estimating program run times - task assignment and scheduling - classical uniprocessor scheduling algorithms - uniprocessor scheduling of IRIS tasks - tasks assignment - mode changes - fault tolerant scheduling.

UNIT II PROGRAMMING LANGUAGES AND TOOLS 9

Language features - desired language characteristics - data typing - control structures - facilitating hierarchical decomposition - package - run-time error handling - overloading and generics - multitasking - low level programming - task scheduling - timing specifications - programming environments - run-time support – code generation.

UNIT III REAL TIME DATABASES 9

Real time database - basic definition - real time Vs general-purpose database - main memory databases - transaction priorities - transaction aborts - concurrency control issues - disk scheduling algorithms - two-phase approach to improve predictability - maintaining serialization consistency - databases for hard real time systems.

UNIT IV COMMUNICATION 9

Real time communication - communications media - network topologies - protocols – buffering data – synchronization – dead lock – mail boxes and semaphores - fault tolerance techniques - fault types - fault detection - fault error containment - redundancy -data diversity - reversal checks - integrated handling.

UNIT V EVALUATION TECHNIQUES 9

Reliability evaluation techniques - reliability models for hardware redundancy - software error models – response time calculation – interrupt latency – time loading and its measurement – reducing response times – analysis of memory requirements – reducing memory loading

TOTAL: 45 HOURS

TEXT BOOK:

1. C.M.Krishna, Kang G. Shin, Real - Time Systems, McGraw-Hill International Editions, 2008.

REFERENCES:

1. Stuart Bennett, Real Time Computer Control -An Introduction, PHI, 1988.

2. Peter D Lawrence, Real Time Micro Computer System Design -An Introduction, McGraw-Hill, 1988.

3. S.T.Allworth and R.N.Zobel, Introduction to real time software design, Macmillan, II Edition, 1987.

4. Real time systems design and analysis - An Engineers handbook 2nd edition - phillip A.Laplante, IEEE Press, IEEE Computer Society Press, 2001

	ELECTIVE	L	T	P	C
	VLSI SIGNAL PROCESSING	**3**	**0**	**0**	**3**

AIM:

To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:

At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I INTRODUCTION TO DSP SYSTEMS 9

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II RETIMING 9

Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III FAST CONVOLUTION 9

Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS 9

Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low

power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL: 45 HOURS

REFERENCES:

1. Keshab K.Parhi, " VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, 'Practical Low Power Digital VLSI Design,' Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	LOW POWER VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.

OBJECTIVE:

At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I

SIMULATION & PROBABILISTIC POWER ANALYSIS **9**

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II
CIRCUIT, LOGIC & SPECIAL TECHNIQUES **9**

Circuit -Logic - Special Techniques - Architecture and Systems.

UNIT III
ADVANCED TECHNIQUES & PHYSICS OF POWER DISSIPATION **9**

Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices.

UNIT IV
POWER ESTIMATION & SYNTHESIS FOR LOW POWER **9**

Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits.

UNIT V
STATIC RAM & SOFTWARE DESIGN FOR LOW POWER **9**

Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques - Software Design for Low Power.

TOTAL: 45 HOURS

REFERENCES:

1. Gary Yeap " Practical Low Power Digital VLSI Design",1997.
2. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", 2000.

	ELECTIVE	L	T	P	C
	MOBILE COMPUTING	**3**	**0**	**0**	**3**

AIM:

The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:

At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT I INTRODUCTION **9**

Basics of mobile computing - Medium access control – Telecommunication systems – Satellite systems – Broadcast systems.

UNIT II STANDARDS **9**

Wireless LAN – IEEE 802.11 – Frequency Hopping spread spectrum – Direct sequence and spread spectrum - HIPERLAN – Bluetooth.

UNIT III ADHOC NETWORKS **9**

Characteristics – Performance issues – Routing in mobile hosts – Destination sequence distance vector – Dynamic source routing – Hierarchical Algorithms.

UNIT IV NETWORK ISSUES **9**

Mobile IP – DHCP – Mobile transport layer – Indirect TCP – Snooping TCP – Transmission / time-out freezing – Selective retransmission – Transaction oriented TCP.

UNIT V APPLICATION ISSUES **9**

Wireless application protocol – Dynamic DNS - File systems – Synchronization protocol – Context-aware applications – Security – Analysis of existing wireless network.

TOTAL: 45 HOURS

REFERENCES:

1. J. Schiller, Mobile Communications, Addison Wesley, 2000.
2. William C.Y.Lee, Mobile Communication Design Fundamentals, John Wiley, 1993.

	ELECTIVE	L	T	P	C
	DIGITAL CONTROL SYSTEMS	**3**	**0**	**0**	**3**

AIM:

To use modern engineering tools, software and equipments to analyze problems.

OBJECTIVE:

- To learn the fundamental principles of feedback control and dynamic systems
- To acquire the concepts of Optimal Control Systems and Digital Control Systems
- To Model and control hybrid systems
- To learn how to perform the stability analysis of Feedback Control Systems

Unit I

Introduction to Control Systems **9 Hours**

Brief History of Automatic Control - Engineering Design - Control System Design - Differential Equations of Physical Systems - Linear Approximations of Physical Systems - The Transfer Function of Linear Systems - The State Variables of a Dynamic System - The State Differential Equation - The Transfer Function from the State Equation - The Time Response and the State Transition Matrix

Unit II

Feedback Control System **9 Hours**

Introduction - Error Signal Analysis - Sensitivity of Control Systems to Parameter Variations – Disturbance Signals in a Feedback Control System - Control of the Transient Response - Steady-State Error - The Cost of Feedback - Test Input Signals - Performance of Second-Order Systems - Effects of a Third Pole and a Zero on the Second-Order System Response - The s-Plane Root Location and the Transient Response – The Steady-State Error of Feedback Control Systems - Performance Indices

Unit III

The Stability of Linear Feedback Systems **9 Hours**

The Concept of Stability - The Routh—Hurwitz Stability Criterion - The Relative Stability of Feedback Control Systems - The Stability of State Variable Systems - The Root Locus Concept - The Root Locus Procedure - Sensitivity and the Root Locus - PID Controllers - Negative Gain Root Locus

Unit IV

Frequency Response **9 Hours**

Frequency Response Plots - Frequency Response Measurements - Performance Specifications in the Frequency Domain - Log Magnitude and Phase Diagrams - The Nyquist Criterion - Relative Stability and the Nyquist Criterion - Time-Domain Performance Criteria in the Frequency Domain - PID Controllers in the Frequency Domain - Phase-Lead Design - Phase-Lag Design

Unit V

Sampled-Data Systems **9 Hours**

Introduction - Digital Computer Control System Applications - Sampled-Data Systems - The z-Transform - Closed-Loop Feedback Sampled-Data Systems - Performance of a Sampled-Data, Second-Order System - Closed-Loop Systems with Digital Computer Compensation - The Root Locus of Digital Control Systems - Implementation of Digital Controllers - Design Examples

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

1. Bishop and Dorf, Digital control systems Design, Prentice Hall; 12 edition, 2010
2. Mohammed S. Santina, Allen R. Stubberud, Gene H. Hostetter, Digital control system design, Oxford University Press, 2 edition, 1994
3. Gopal, Digital Control and State Variable Methods, Tata McGraw Hill, 2008