AVIT AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY

VINAYAKA MISSION'S RESEARCH FOUNDATION (Deemed to be University under section 3 of the UGC Act 1956)

Accredited by NAAC

Approved by AICTE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LIST OF EXPERIMENTS

PROG, BRANCH,	**B. E., E. C. E**
YEAR/ SEMESTER, SECTION	**III / VI, -**
SUBJECT	**17ECCC90 – FPGA Systems Lab**
ACADEMIC YEAR	**2020-2021 (EVEN SEMESTER)**

1. Implementation of Logic Gates –Data flow model and Behavioural model
2. Combinational logic circuits –Adders and Subtractor
3. Code converters-Binary to Gray and Gray to Binary
4. 3 to 8 Decoder –74138
5. 4 Bit Comparator –7485
6. 8 x 1 Multiplexer –74151 and 2X4 Demultiplexer –74155
7. 16 x 1 Multiplexer –74150 and 4X16 Demultiplexer –74154
8. Sequential circuits -Flip-Flops
9. Decade counter –7490.
10. Synchronous & Asynchronous Counters
11. Shift registers –7495.
12. Universal shift registers –74194/195.
13. RAM (16 x 4) –74189 (Read and Write operations).
14. Stack and Queue Implementation using RAM

HOD/ ECE