VINAYAKA MISSIONS RESEARCH FOUNDATION
AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR
TIMETABLE
Ref.No: AVIT/TT/03

SEMESTER: ODD **ACADEMIC YEAR : 2021-2022**

DEPT : EEE **DATE : 26.08.2021**

Venue : Digital Logic Circuits & Design Lab **With Effect From : 6.9.2021**

Lab Head: Mrs.S.Jensie Anita

Day/ Period	1	2	MORNING BREAK (11:00A.M -11:15A.M)	3	LUNCH BREAK (12.15 P.M. - 1.00 P.M.)	4	5	AFTERNOON BREAK (2:55 P.M -3.05 P.M)	6
	9:00-10.00	10.00-11.00		11.15-12.15		1:00 - 2:00	2.00 - 2.55		3.05-4.00
Monday									
Tuesday						DLCD Lab			DLCD Lab
Wednesday									
Thursday									
Friday									

S.NO	MNEMONIC	COURSE CODE	COURSE TITLE	Sem. / Branch	NAME OF THE FACULTY
1	DLCD Lab	17ECCC82	Digital Logic Circuits & Design Lab	II / MECT	Mrs.D.Saranya

TIME TABLE COORDINATOR **HOD**