VINAYAKA MISSION’S RESEARCH FOUNDATION
AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

LAB MANUAL

SEMICONDUCTOR DEVICES LAB

CLASS: III SEMESTER

(MECHATRONICS)

REGULATION 2017

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SYLLABUS
SEMESTER III
SEMICONDUCTOR DEVICES LAB

List of Experiments

1. Half wave rectifier.
2. Full wave rectifier.
3. Clipper
4. Clamper
5. Input, Output characteristics of CE Amplifier.
6. Input, Output characteristics of CC Amplifier.
7. Transfer characteristics of JFET.
8. Voltage Regulator.
9. TRIAC, DIAC
10. SCR.

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HOD/ EEE
Dr. L. Chitra

Exp. No: 1

HALF WAVE RECTIFIER

AIM:

To construct a half-wave rectifier using diode and draw its performance characteristics.

APPARATUS REQUIRED:

S. No	Name	Range	Qty
1.	Transformer	230/(9-0-9)	1
2.	Diode	IN4007	1
3.	Resistor	1KΩ	1
4.	Bread Board	-	1
5.	Capacitor	100µf	1
6.	CRO	-	1

FORMULAE:

WITHOUT FILTER:

(i) $V_{rms} = V_m / \sqrt{2}$

(ii) $V_{dc} = V_m / \pi$

(iii) Ripple Factor $= \sqrt{(V_{rms} / V_{dc})^2 - 1}$

(iv) Efficiency $= (V_{dc} / V_{rms}) \times 100$

WITH FILTER:

(i) $V_{rms} = \sqrt{(V_{rms}'^2 + V_{dc}^2)}$

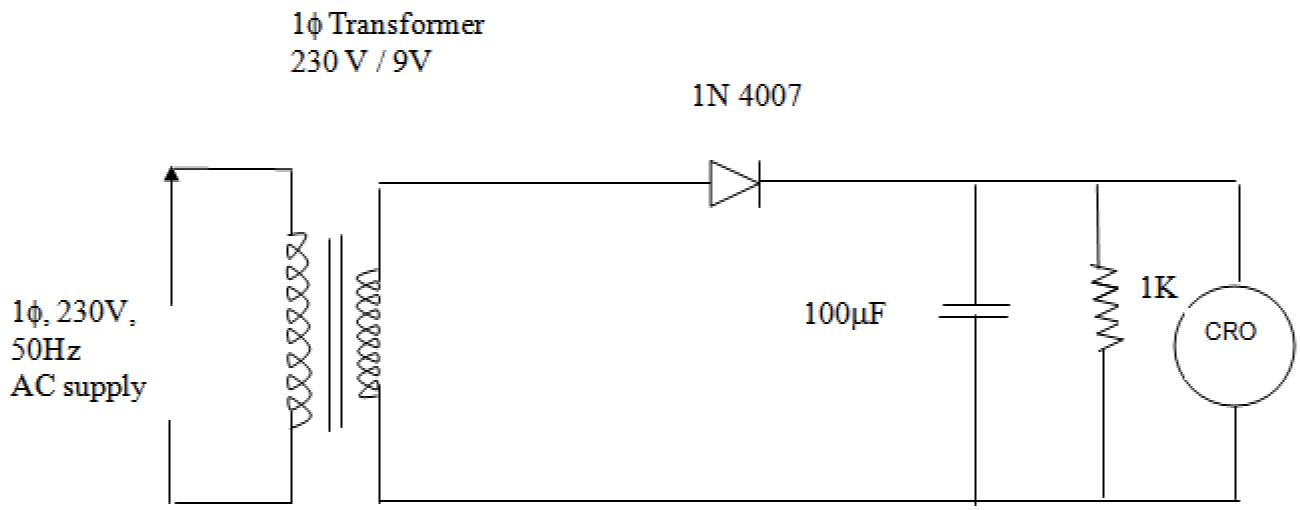
(ii) $V_{rms}' = V_{rpp} / (2 * \sqrt{3})$

(iii) $V_{dc} = V_m - V_{rpp} / 2$

(iv) Ripple Factor $= V_{rms}' / V_{dc}$

CIRCUIT DIAGRAM:

With filter:



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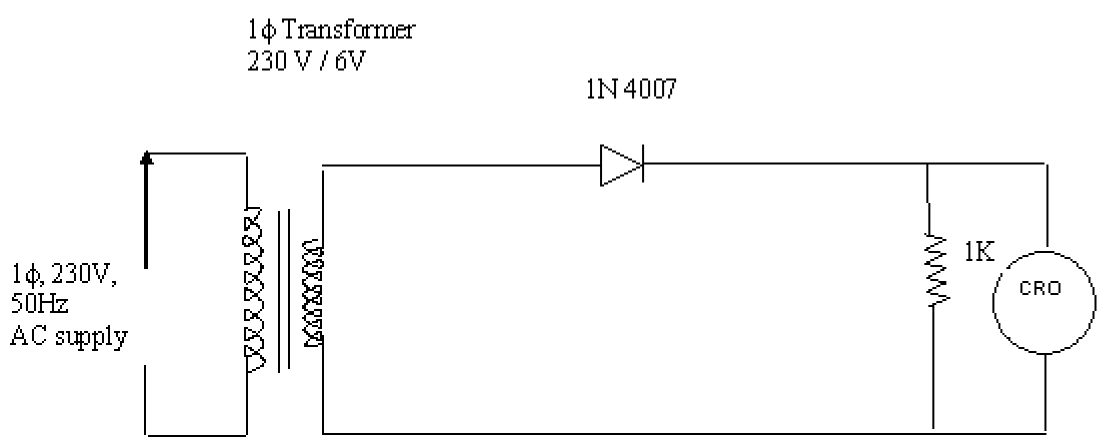


TABULAR COLUMN:

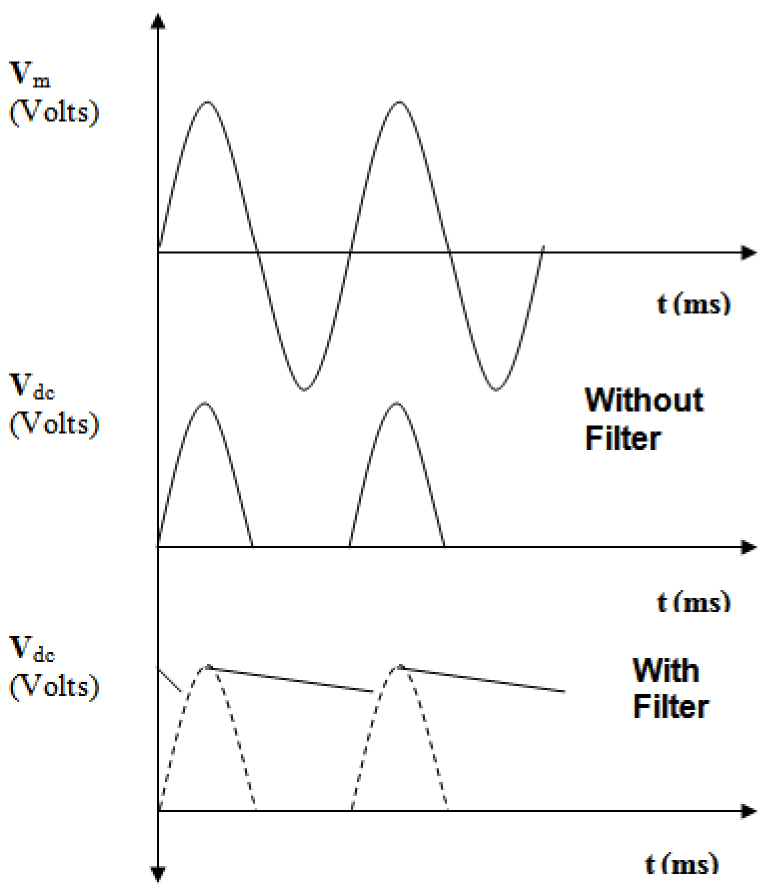
WITHOUT FILTER:

V_m (v)	V_{rms} (v)	V_{dc} (v)	Ripple factor	Efficiency

WITH FILTER:

V_{rms} (v)	V_{rpp}(v)	V_{dc}(v)	Ripple factor

MODEL GRAPH:



PROCEDURE:

WITHOUT FILTER:

1. Connections are given as per the circuit diagram.
2. Give 230v, 50HZ I/P to the step down TFR where secondary connected to the Rectifier I/P.
3. Take the rectifier output across the Load.
4. Plot its performance graph.

WITH FILTER:

1. Connections are given as per the circuit diagram.
2. Give 230v, 50HZ I/P to the step down TFR where secondary connected to the Rectifier I/P.
3. Connect the Capacitor across the Load.
4. Take the rectifier output across the Load.
5. Plot its performance graph.

RESULT:

Thus the performance characteristic of 1ϕ half wave rectifier was obtained.

Exp. No: 2

FULL WAVE RECTIFIER

AIM:

To construct a Full wave rectifier using diode and to draw its performance characteristics.

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1.	Transformer	230/(9-0-9)	1
2.	Diode	IN4001	2
3.	Resistor	1KΩ	1
4.	Bread Board	-	1
5.	Capacitor	100µf	1
6.	CRO	-	1

FORMULAE:

WITHOUT FILTER:

(i) V_{rms} = $V_m / \sqrt{2}$

(ii) V_{dc} = $2V_m / \prod$

(iii) Ripple Factor = $\sqrt{((V_{rms} / V_{dc})^2 - 1)}$

(iv) Efficiency = (V_{dc} / V_{rms}) x 100

WITH FILTER:

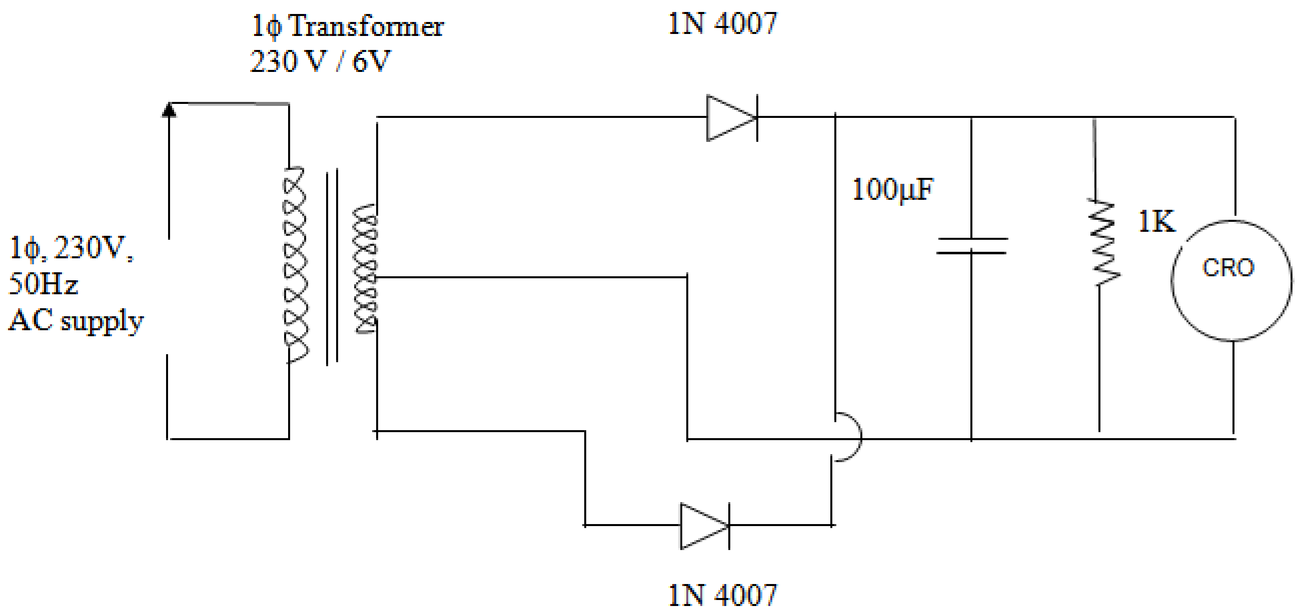
(i) V_{rms} = $V_{rpp} / (2*\sqrt{3})$

(ii) V_{dc} = $V_{m} - V_{rpp}$

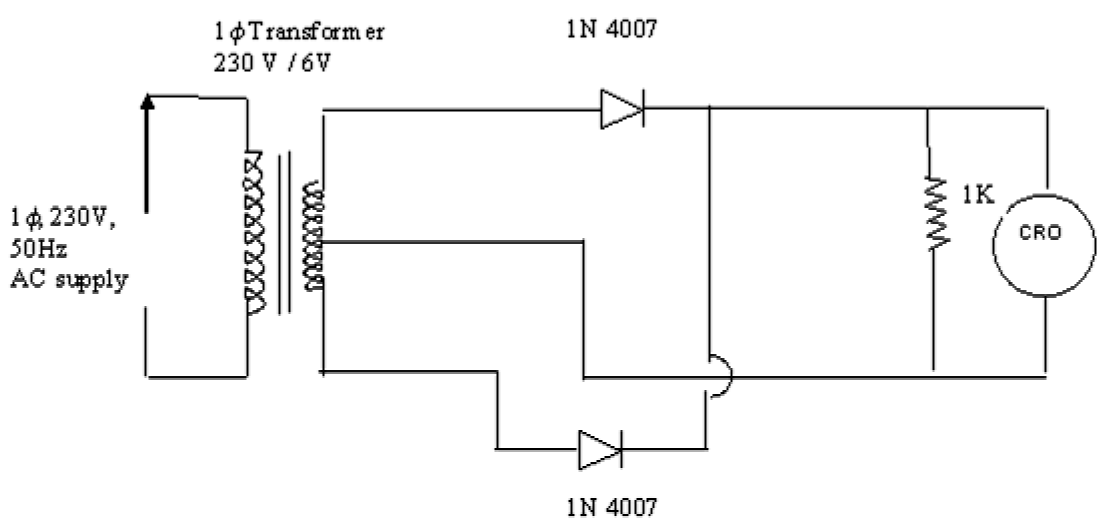
(iv) Ripple Factor = $V_{rms'} / V_{dc}$

CIRCUIT DIAGRAM

With Filter



Without Filter



TABULAR COLUMN:

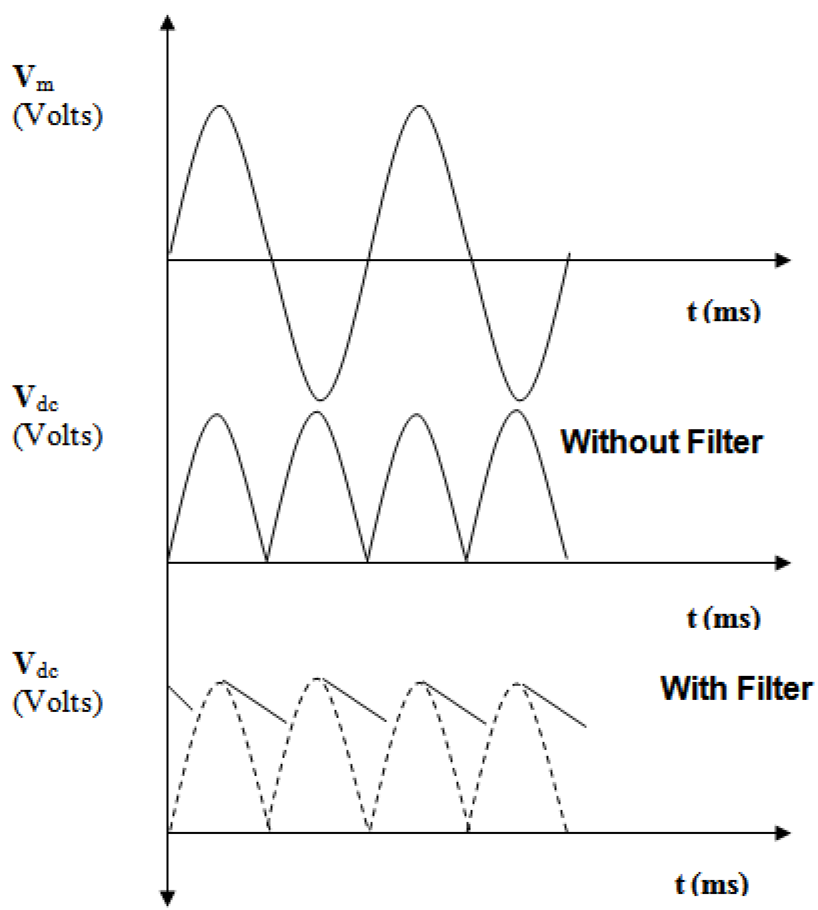
WITHOUT FILTER:

V_m (V)	V_{rms} (V)	V_{dc} (V)	Ripple factor	Efficiency

WITH FILTER:

V_{rms} (V)	V_{rpp} (V)	V_{dc} (V)	Ripple factor

MODEL GRAPH



PROCEDURE:

WITHOUT FILTER:

1. Connections are given as per the circuit diagram.
2. Give 230v, 50HZ I/P to the step down TFR where secondary connected to the Rectifier I/P.
3. Take the rectifier output across the Load.
4. Plot its performance graph.

WITH FILTER:

1. Connections are given as per the circuit diagram.
2. Give 230v, 50HZ I/P to the step down TFR where secondary connected to the Rectifier I/P.
3. Connect the Capacitor across the Load.
4. Take the rectifier output across the Load.
5. Plot its performance graph.

RESULT:

Thus the performance characteristics of 1ϕ Full wave rectifier were obtained.

Exp. No: 3

CLIPPER

AIM:

To construct a Clipper using diode and to draw its performance characteristics.

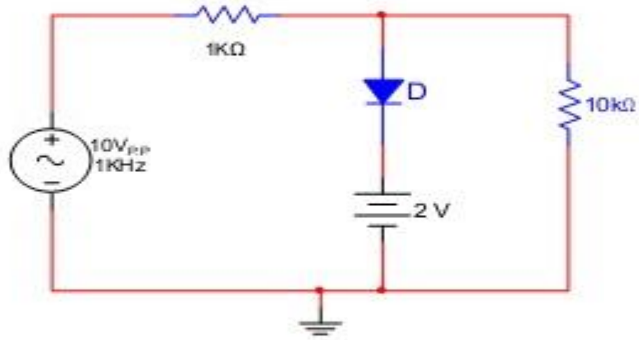
APPARATUS REQUIRED:

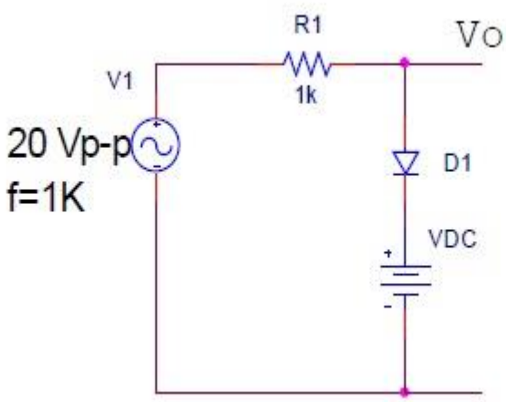
S.No	Name	Range	Qty
1.	Function Gen	-	1
2.	Diode	IN4001	2
3.	Resistor	1KΩ	1
4.	Bread Board	-	1
5.	Capacitor	100µf	1
6.	CRO	-	1

Theory:

clipper circuits have the ability to “clip” off a portion of the input signal without distorting the remaining part of the alternating waveform. The half wave rectifier of the previous experiment is an example of the simplest form of diode clipper. Depending on the orientation of thy diode, the positive or negative region of the input signal is “clipped” off. There are two general categories of clippers: series and parallel. The series c configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in branch parallel to the load.

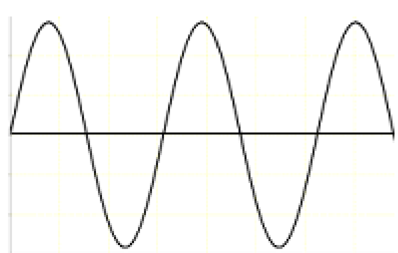
Circuit Diagram:



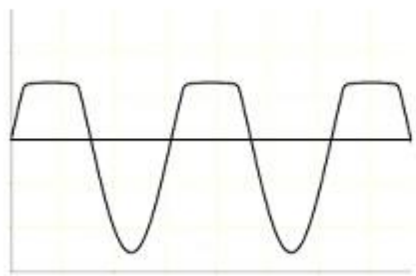


Model Graph:

Input Characteristics:



Output Characteristics:



Procedure:

Clipping Circuit:

1. Connect the circuit shown in Figure.

2. Ensure that the variable DC is at minimum and the source is at 10VP.P.

3. Observe and Sketch the input and output waveforms.

4. Increase the variable DC voltage to 4V, and notice to what voltage are the Positive peaks chopped off, sketch the waveforms.

Result:

Thus the static characteristics clipper configuration studied.

Exp. No: 4

CLAMPER

AIM:

To construct a Clamper using diode and to draw its performance characteristics.

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1.	Function Gen	-	1
2.	Diode	IN4001	2
3.	Resistor	1KΩ	1
4.	Bread Board	-	1
5.	Capacitor	100µf	1
6.	CRO	-	1

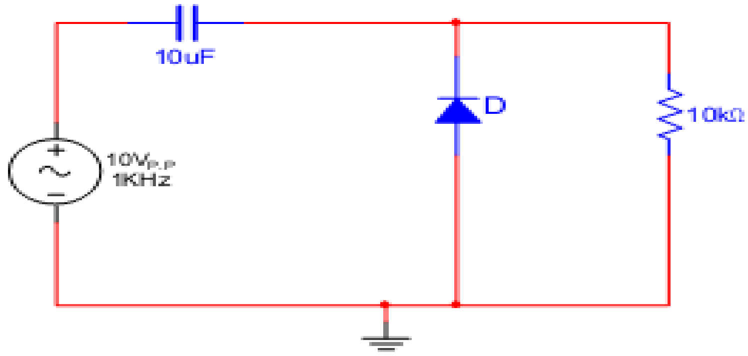
Theory:

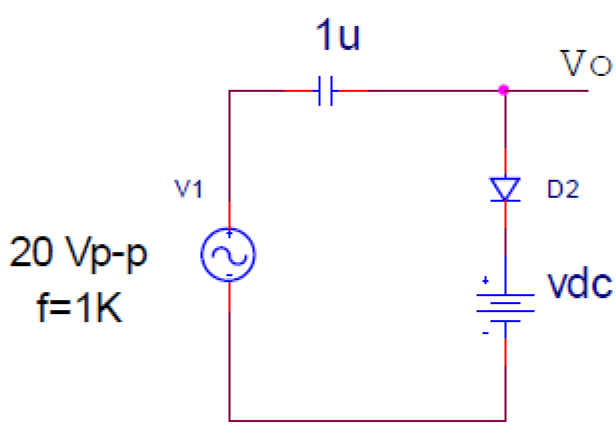
Sometimes you may want to leave the waveform unchanged, but modify its DC level up or down. To accomplish this, you use a clamper circuit. The beauty of clampers is that they can adjust the DC position of the waveform without knowing what the waveform actually is. The positive clamper shown in the figure below works as follows:

In the positive half of the first cycle, the voltage across the capacitor cannot change instantaneously; therefore as the voltage on the input moves up, the voltage on the top of the diode has to follow this voltage. This reverse biases the diode causing it to act as an open, thus the output voltage follows the input voltage. As the input voltage drops into the negative half of the first cycle, the diode is going to be forward biased. In the positive half of the first cycle, the voltage across the capacitor cannot change instantaneously; therefore as the voltage on the input moves up, the voltage on the top of the diode has to follow this voltage.

This reverse biases the diode causing it to act as an open, thus the output voltage follows the input voltage. As the input voltage drops into the negative half of the first cycle, the diode is going to be forward biased. This causes the diode to behave like a wire, which cannot dissipate any voltage. This causes to inter-related effects. First, the output voltage is held steady at 0V. Second, because there are 0V dissipated across the diode (and resistor) all of the voltage has to be dissipated across the capacitor. This charges the capacitor to the magnitude of the input signal.

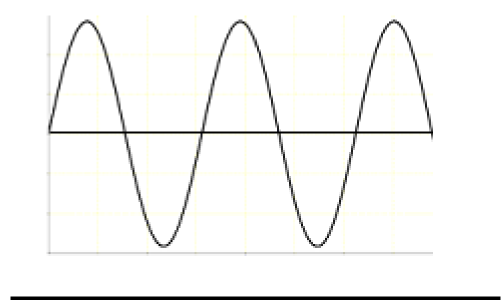
Circuit Diagram:



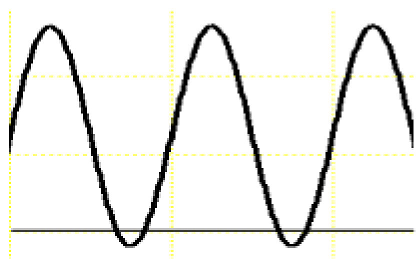


Model Graph:

Input Characteristics:



Output Characteristics:



Procedure:

Clamping Circuit:

1. Connect the circuit shown in Figure.

2. Ensure the variable DC is at minimum.

3. Set the sine wave generator frequency to 1KHz and its output amplitude to 10VP.P

4. Observe and sketch the input waveform with the variable DC at minimum,

5. Sketch the output waveform.

Result:

Thus the static characteristics clamper configuration studied.

EXP. NO: 5

INPUT AND OUTPUT CHARACTERISTICS BJT (CE CONFIGURATION)

Aim:

To obtain the input and output Characteristics of Common Emitter configuration

Apparatus and Components Required:

S.No	Name of the Apparatus	Range/No/Type	Quantity
1	Transistor	BC107	1
2	Voltmeter	0-2V,0-30V	Each1
3	Ammeter	0-500µA, 0-30mA,	Each 1
4	DC Power Supply (Dual)	0-30V	1
5	Breadboard		1
6	Resistors	1k,10k,	Each 1
7	Connecting Wires		As required

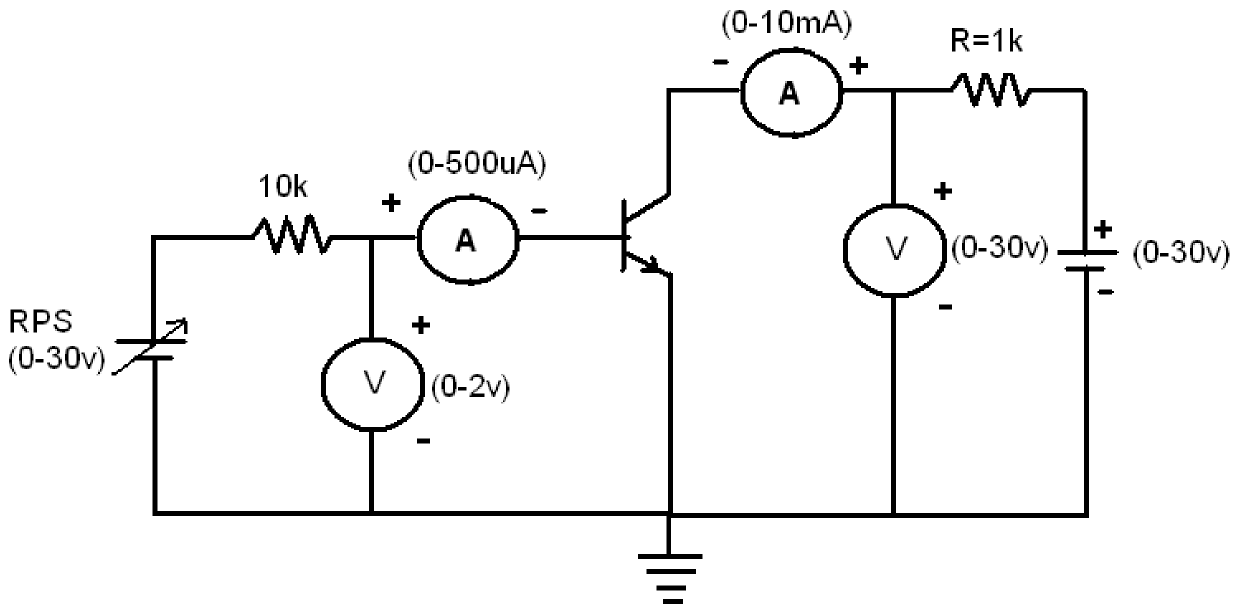
Theory:

The transistor is a semiconductor device having three terminals called Emitter, Base and Collector. It consists of two diodes namely, emitter-base diode and collector-base diode connected back to back, BJT is classified in to NPN and PNP transistor and doping varies between the three layers.

In BJT (Bipolar Junction Transistor) current conduction takes place by both minority and majority charge carriers. It also called current controlled device, because the output current is controlled by its input current, The external DC biasing is applied to the transistor to fix the Q – point in any one of the region out of three region ie. active, Cut-off and saturation region, used for different applications. Always the emitter-base junction is forward biased and collector to base is reverse biased and Q – point is fixed on center of DC load line(In active region) to operate transistor as an amplifier.

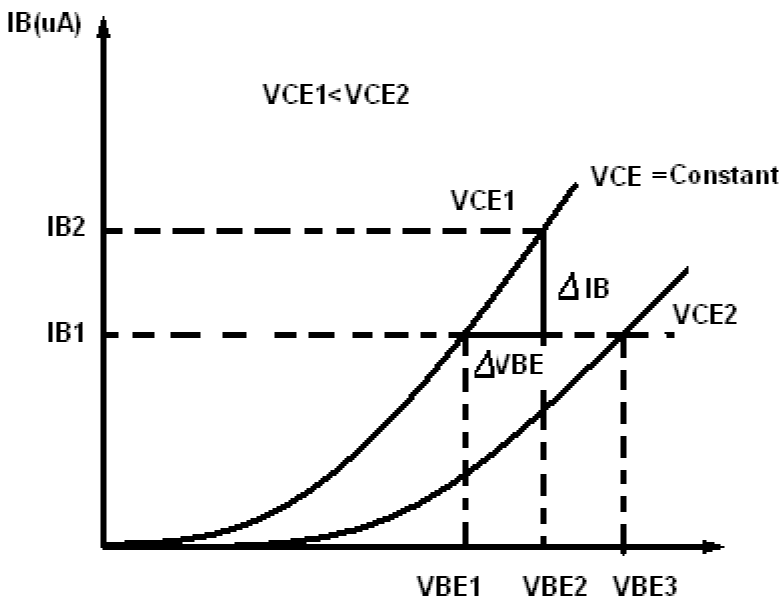
There are three possible arrangements (configuration) for investigating its DC Characteristics. From each of these configurations three sets of characteristics may be derived, there are the input characteristics, Output characteristics and Current gain characteristics.

Circuit Diagram:

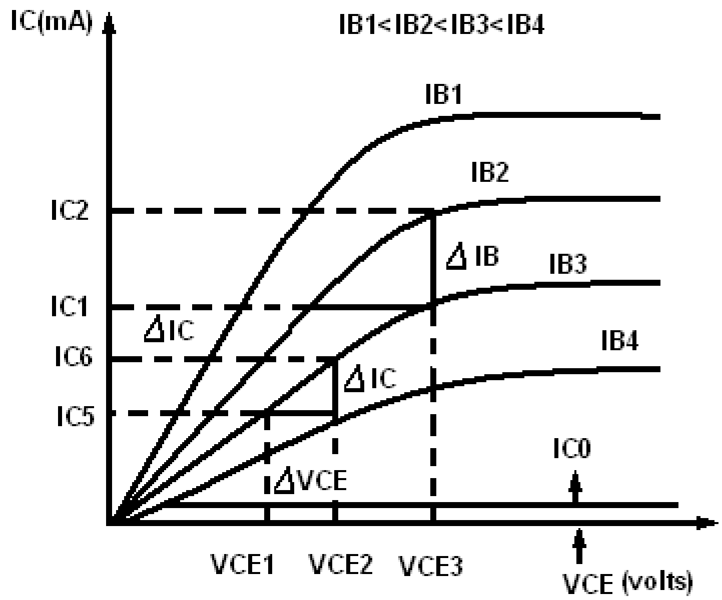


Model Graph:

Input Characteristics:



Output Characteristics:



Tabulation:

Input Characteristics:

V_{CE} (V)		V_{CE} (V)	
V_{BE} (V)	**I_B (μA)**	**V_{BE} (V)**	**I_B (μA)**

Output Characteristics:

I_B (μA)		I_B (μA)	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)

Procedure:

Input Characteristics:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CE} = 5V, vary, V_{BE} insteps of 0.1V & note down the corresponding I_B and repeat the above procedure for 10V & so on.
3. Plot the graph: V_{BE} vs I_B for a constant V_{CE}.
4. Find the h-parameters: hfe & hie.

Output Characteristics:

1. Connect the circuit as per the circuit diagram.
2. Set I_B = 20μA, vary V_{CE} insteps of 1V & note down the corresponding I_C . Repeat the above procedure for 40μA,80μA & so on.
3. Plot the graph: V_{CE} vs I_C for a constant of I_B .
4. Find the h-parameters: hoe & hre.

Result:

Thus the static characteristics of transistor in Common Emitter configuration studied.

EXP. NO: 6

INPUT AND OUTPUT CHARACTERISTICS BJT (CC CONFIGURATION)

Aim:

To obtain the input and output Characteristics of Common Collector configuration

Apparatus and Components Required:

S.No	Name of the Apparatus	Range/No/Type	Quantity
1	Transistor	BC107	1
2	Voltmeter	0-2V,0-30V	Each1
3	Ammeter	0-500µA, 0-30mA,	Each 1
4	DC Power Supply (Dual)	0-30V	1
5	Breadboard		1
6	Resistors	1k,10k,	Each 1
7	Connecting Wires		As required

Theory:

A BJT is a three terminal two – junction semiconductor device in which the conduction is due to both the charge carrier. Hence it is a bipolar device and it amplifier the sine waveform as they are transferred from input to output. BJT is classified into two types – NPN or PNP. A NPN transistor consists of two N types in between which a layer of P is sandwiched. The transistor consists of three terminal emitter, collector and base. The emitter layer is the source of the charge carriers and it is heartily doped with a moderate cross sectional area. The collector collects the charge carries and hence moderate doping and large cross sectional area. The base region acts a path for the movement of the charge carriers. In order to reduce the recombination of holes and electrons the base region is lightly doped and is of hollow cross sectional area. Normally the transistor operates with the EB junction forward biased.

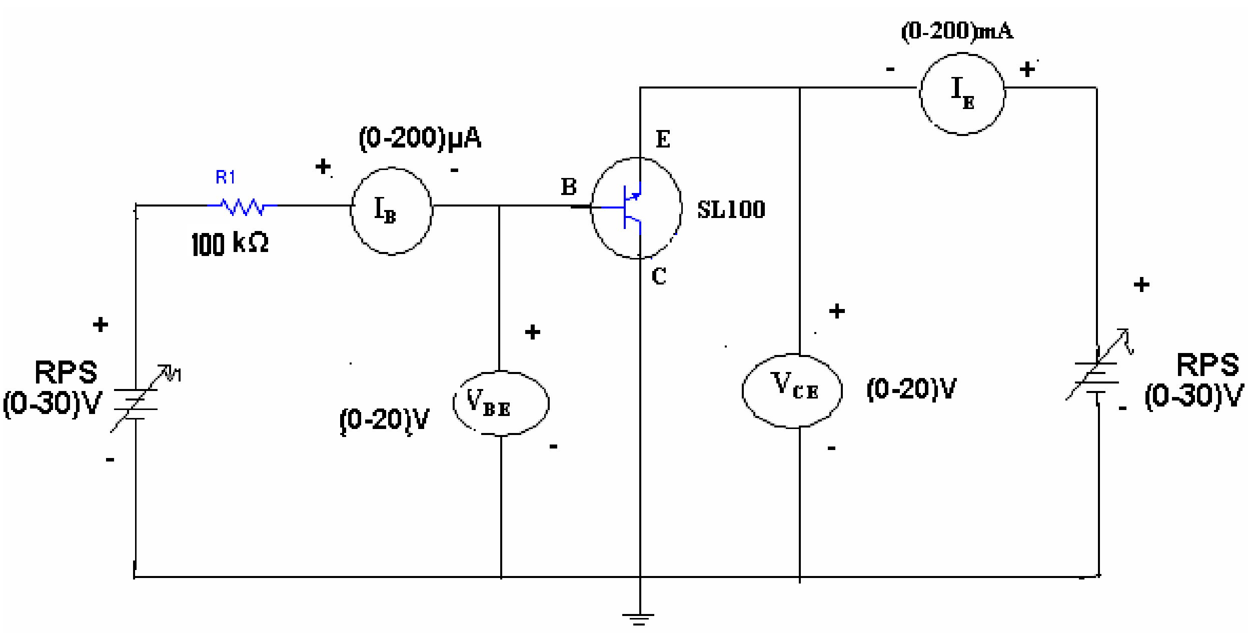
In transistor, the current is same in both junctions, which indicates that there is a transfer of resistance between the two junctions. One to this fact the transistor is known as transfer resistance of transistor

In this configuration we use collector terminal as common for both input and output signals. This configuration is also known as emitter follower configuration because the emitter voltage follows the base voltage. This configuration is mostly used as a buffer. These configurations are widely used in impedance matching applications because of their high input impedance.

In this configuration the input signal is applied between the base-collector region and the output is taken from the emitter-collector region. Here the input parameters are VBC and IB and the output parameters are VEC and IE. The common collector configuration has high input impedance and low output impedance. The input and output signals are in phase. Here also the emitter current is equal to the sum of collector current and the base current. Now let us calculate the current gain for this configuration.

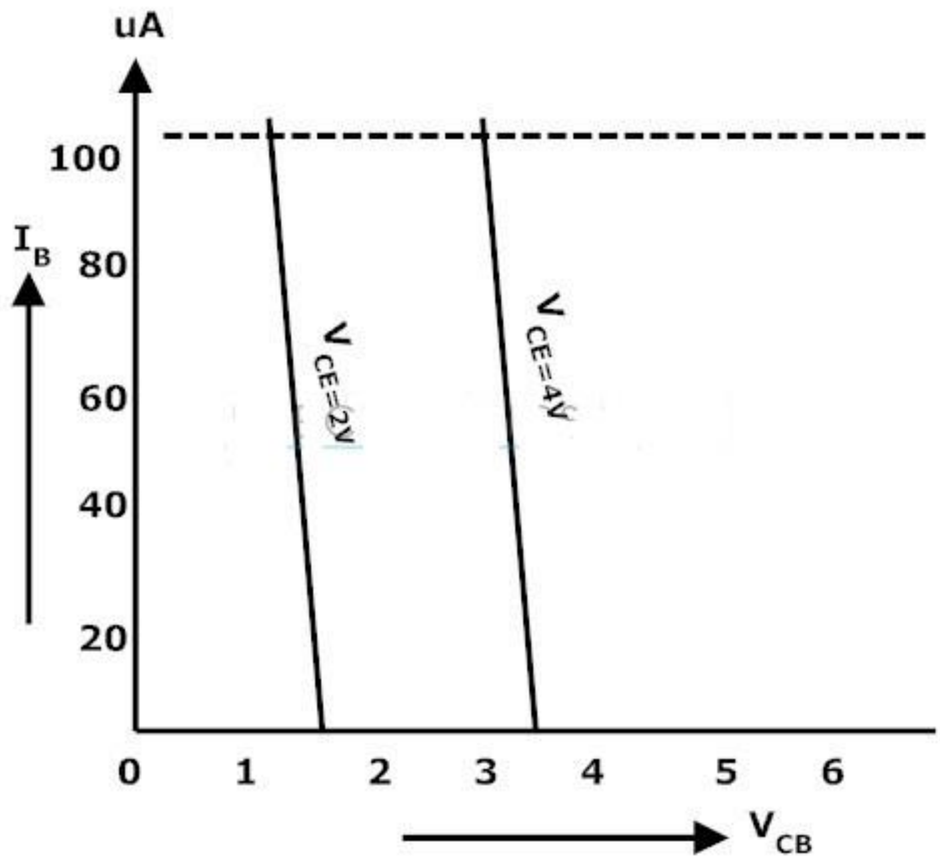
This common collector configuration is a non-inverting amplifier circuit. The voltage gain for this circuit is less than unity but it has large current gain because the load resistor in this circuit receives both the collector and base currents.

Circuit Diagram:

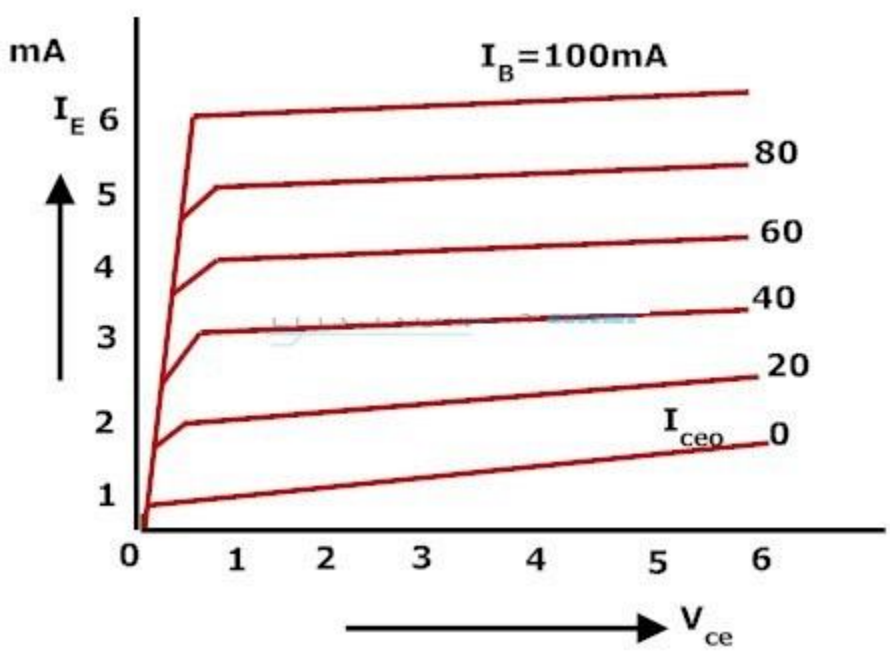


Model Graph:

Input Characteristics:



Output Characteristics:



Tabulation:

Input Characteristics:

V_{CE} (V)=		V_{CE} (V)=	
V_{CB} (V)	I_B (μA)	V_{CB} (V)	I_B (μA)

Output Characteristics:

I_B (μA)=		I_B (μA)=	
V_{CE} (V)	I_E (mA)	V_{CE} (V)	I_E (mA)

Procedure:

Input Characteristics:

1. Connect the circuit as per the circuit diagram.
2. Set V_{CE} = 5V, vary, V_{BE} insteps of 0.1V & note down the corresponding I_B and repeat the above procedure for 10V & so on.
3. Plot the graph: V_{CB} vs I_B for a constant V_{CE}.
4. Find the h-parameters: hfc & hic.

Output Characteristics:

1. Connect the circuit as per the circuit diagram.
2. Set I_B = 20µA, vary V_{CE} insteps of 1V & note down the corresponding I_E . Repeat the above procedure for 40µA,80µA & so on.
3. Plot the graph: V_{CE} vs I_C for a constant of I_B .
4. Find the h-parameters: hoc & hrc.

Result:

Thus the static characteristics of transistor in Common Emitter configuration studied.

Exp. No: 7

TRANSFER CHARACTERISTICS OF JFET

Aim:

To obtain the Drain and Transfer characteristics of JFET

Apparatus and Components Required:

S. No	Name of the Apparatus	Range/No/Type	Quantity
1	JFET(Junction Field Effect Transistor)	BFW10	1
2	Voltmeter	0-30V,0-5V	Each1
3	Ammeter	0-10mA	1
4	DC Power Supply (Dual)	0-30V	1
5	Breadboard		1
6	Resistors	33KΩ,1KΩ	Each 1
7	Connecting Wires		As required

Theory:

Like a bipolar junction transistor, a field effect transistor is also a three terminal which are source, drain and gate. FET is also called as uni-polar device because its function depends only upon the one type of carrier ie. Due to either majority or minority charge carriers. It is also called voltage control device, because the output current is controlled by its input voltage.

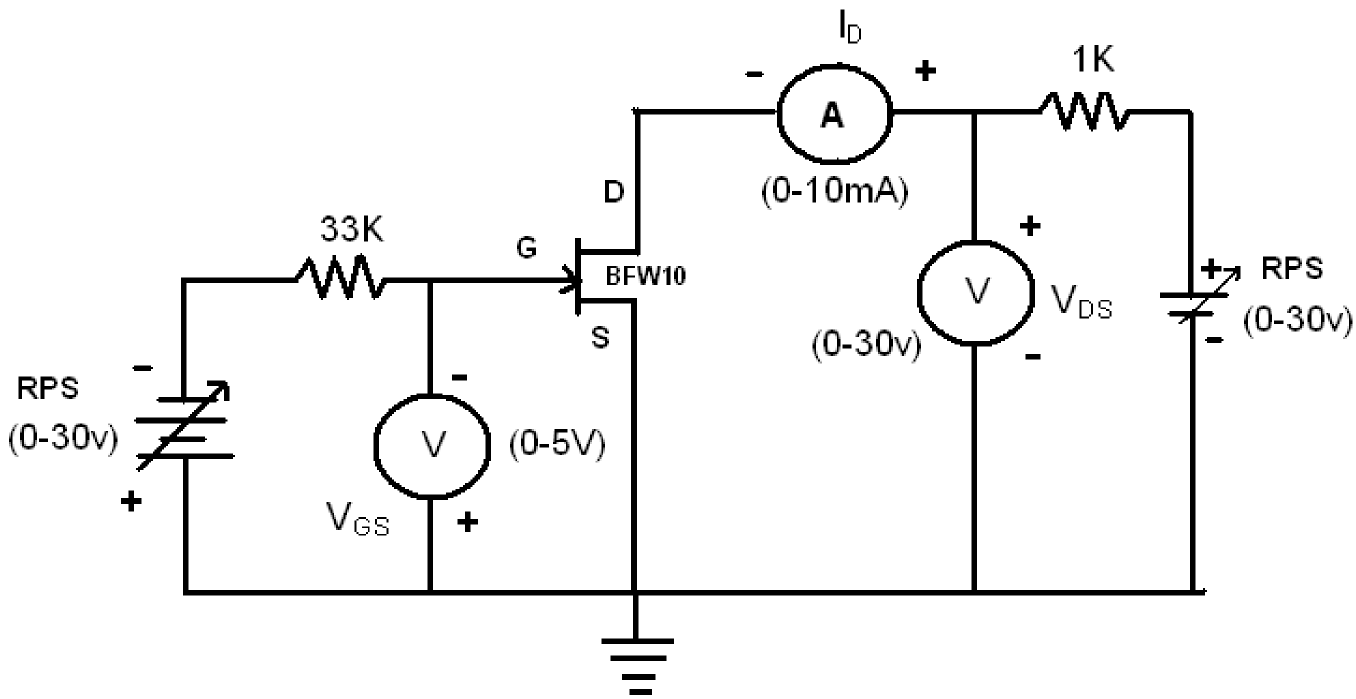
A field effect transistor can be either a JFET of MOSFET. Again a JFET can either have n-channel or p-channel. An n-channel has an n-type semiconductor bar. The two ends of which the drain and source terminal on the two side of this bar, PN junction are made. This p-region makes gates. Usually the two gates are connected together to form a single gate. The gate is given a negative bias with respect to the source. The drain is given positive potential with respect to the source, In case of p-channel JFET the terminal of all the batteries are reversed.

In this case, PN junction is reverse bias and the thickness of the depletion region increases. As V_{GS} is decreased from zero, drain is positive with respect to the source with V_{GS} = 0. Now majority carriers flow through the n-channel from source to drain. Therefore the conventional current flow from drain to source since the current is controlled by only majority carriers, FET is called as uni-polar device.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse bias voltage applied to the gate. The drain current depends on the drain voltage V_{DS} and the gate voltage V_{GS}. Any of this variables may be fixed and the relation between the other two are determined when V_{DS}=V_P, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch off region are saturation region increases.

Circuit Diagram:

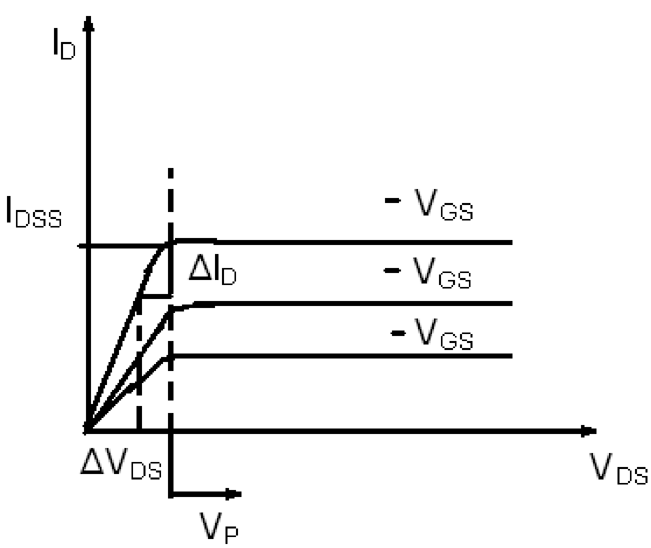
JFET



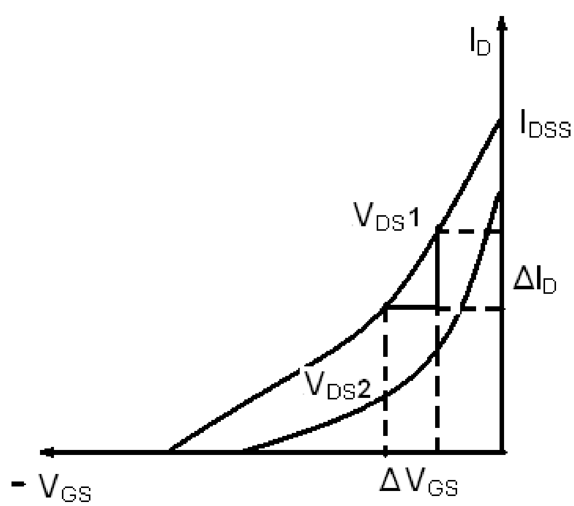
Model Graph:

JFET

Drain Characteristics:



Transfer Characteristics:



Tabulation:

Drain Characteristics:

$-V_{GS} =$ (V)		$-V_{GS} =$ (V)	
V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

Transfer Characteristics:

$V_{DS} =$ (V)		$V_{DS} =$ (V)	
$-V_{GS}$(V)	I_D(mA)	$-V_{GS}$(V)	I_D (mA)

Calculations:

JFET Parameters:

1. DC Drain Resistance (R_{DS})

   $R_{DS} = V_{DS} / I_D$

2. AC Drain Resistance (r_d)

   $r_d = (\Delta V_{DS} / \Delta I_D)$ at constant V_{GS}.

3. Transconductance (G_m)

   $G_m = (\Delta I_D / \Delta V_{GS})$ at constant V_{DS}

4. Amplification Factor (μ)

   $\mu = r_d * G_m$

Procedure:

The connections are given as per the circuit diagram.

Drain characteristics:

1. V_{GS} is kept constant by adjusting the input side power supply.
2. By varying the supply voltage at the output side the corresponding Voltage V_{DS} and Current I_D is noted.
3. Repeat the same procedure for various constant values of V_{GS} .
4. Plot the graph between I_D and $V_{GS.}$

Transfer Characteristics:

1. Drain Voltage V_D is kept constant by adjusting the output side power supply.
2. By Varying the supply at the input side the corresponding voltage V_{GS} and current I_D is noted.
3. Repeat the same procedure for various constant values of $V_{D.}$
4. Plot the Graph between V_{GS} and $I_{D.}$

Result:

Thus the Drain and Transfer Characteristics of JFET has been studied and its parameters are calculated.

- ❖ DC Drain Resistance =
- ❖ AC Drain Resistance =
- ❖ Transconductance =
- ❖ Amplification Factor =
- ❖ Pinch off Voltage =
- ❖ I_{DSS} =

Exp. No:8

VOLTAGE REGULATION USING ZENER DIODE

AIM:

To obtain Voltage regulation using Zener Diode.

APPARATUS REQUIRED:

S. No.	Name	Range	Qty
1	Transistor	SL-100	1
2	Resistor	470Ω	1
3	Zener diode	Z-5.6	1
4	Resistance decade box		1
5	Ammeter	(0-50)mA	1
6	Voltmeter	(0-10)V	1
7	RPS	(0-30)V	1
8	Breadboard		1
9	Connecting wires		As required

THEORY:

ZENER VOLTAGE REGULATION:

Zener current varies over a wide range as input voltage and lower current varies as a result the output voltage which is equal to Vo also changes by small amount. Those changes in the output voltage can be minimized by reducing the change in Zener current with the help of circuit flat emitter follow type regulation.

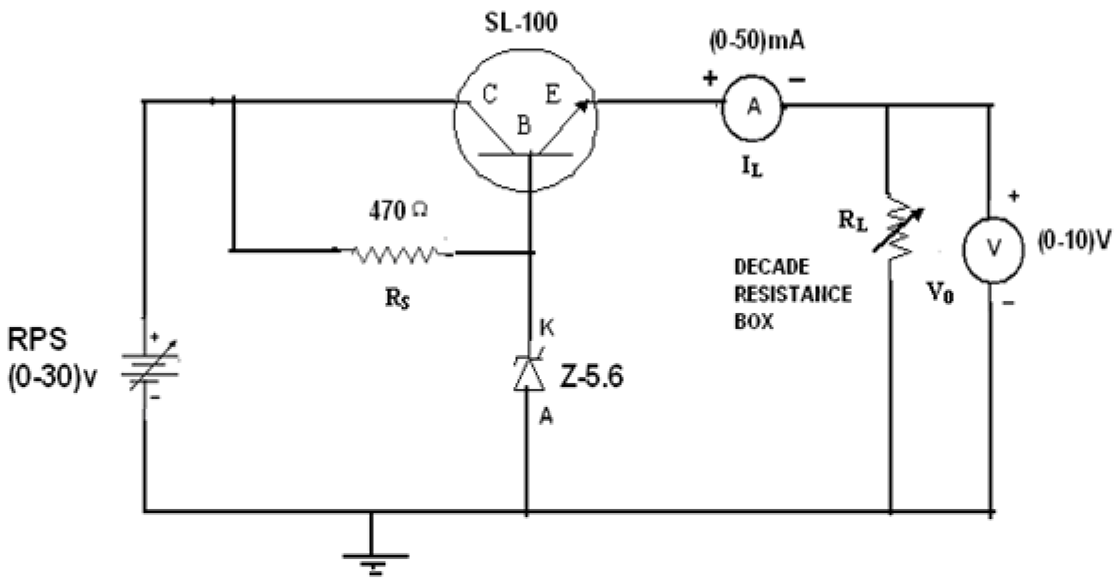
1. When SL is fixed input voltage increases as current input increases.
2. If current through the Zener diode increases without affecting the load current.
3. Increase in input current also increases a voltage that drop in resistance.
4. Input voltage is constant but load current is varies by varying the load resistance.
5. Input is equal to sum of zener current and load current.

i) $\mathbf{I_S = I_Z + I_L}$

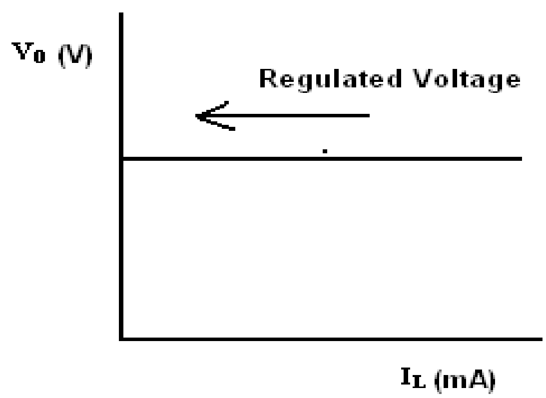
ii) $\mathbf{I_Z = I_S - I_L}$

iii) $\mathbf{I_S = V_S - V_O / R_L}$

CIRCUIT DIAGRAM



MODEL GRAPH:



Ability of power maintains constant output voltage instantaneous A.C input voltage and a change in load resistance.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. For various resistance values Voltage and current are noted.
3. Graph is drawn between I_C and V_O.

RESULT:

Thus the voltage regulation is constructed using Zener diode.

Exp. No: 9

CHARACTERISTICS OF TRIAC, DIAC

AIM:

To obtain the V-I characteristics of TRIAC, DIAC and find the break over voltage and holding current.

APPARATUS REQUIRED:

S. No.	Name	Range	Qty
1	TRIAC	BTM36	1
2	DIAC	SSD3A	1
3	Resistor	330Ω	1
4	Ammeter	(0-50)mA	1
5	Voltmeter	(0-10)V	1
6	RPS	(0-30)V	2
7	Breadboard		1
8	Connecting wires		As required

THEORY:

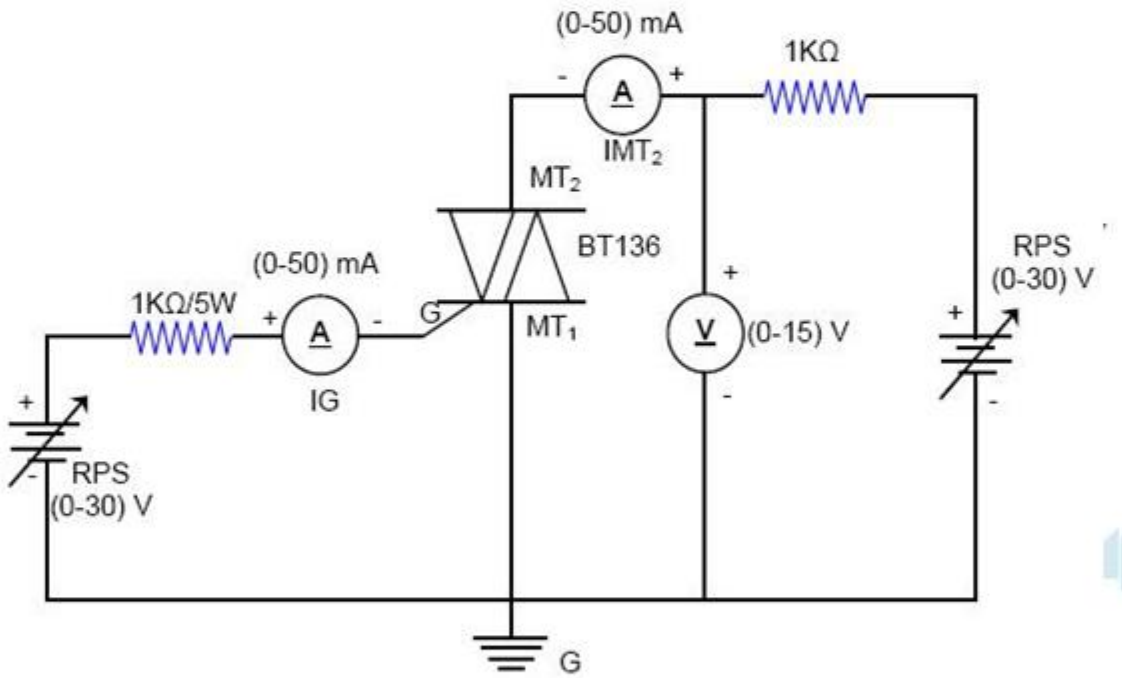
A TRIAC is a three terminal semiconductor switching device which can control alternating current in a load. A TRIAC can control conduction of both positive and negative half cycles of A.C supply. It is sometimes called a bidirectional semiconductor triode switch

A DIAC is a two terminal three layer bidirectional device which can be switched from its off state to on state for either polarity of applied voltage. The operation of DIAC is identical both in forward and reverse conduction. The DIAC does not conduct until the applied voltage of either polarity reaches the break over voltage VBO.

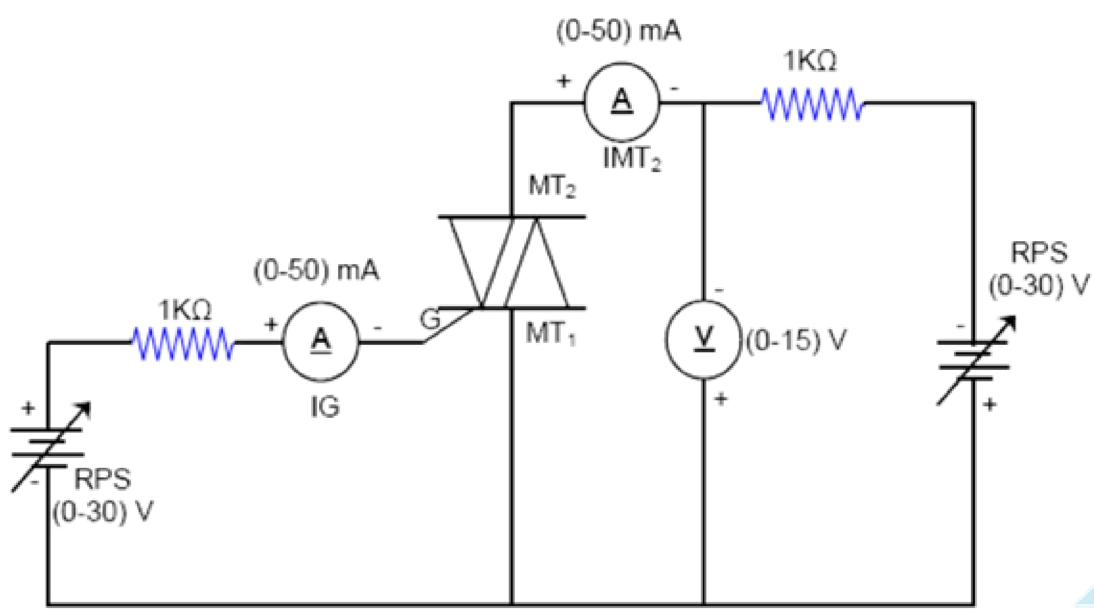
CIRCUIT DIAGRAM

Characteristics of Triac:

Forward Direction:



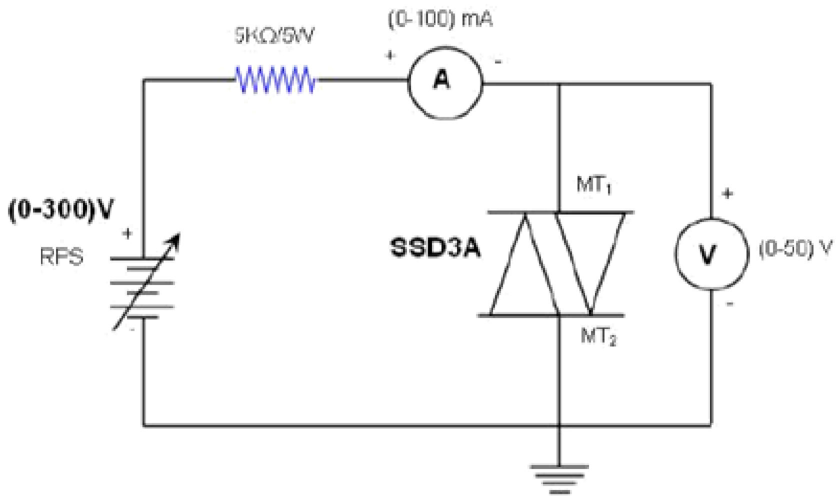
Reverse Direction:



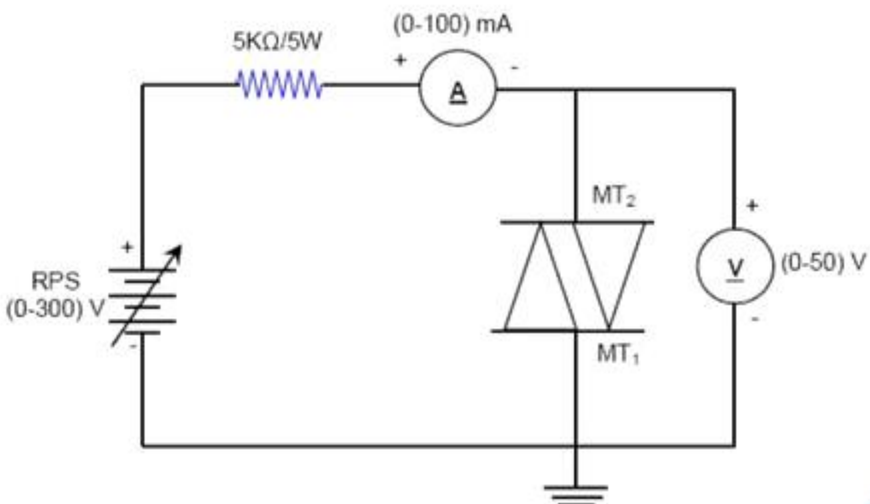
Characteristics of Diac:

Circuit Diagram:

Forward Direction:

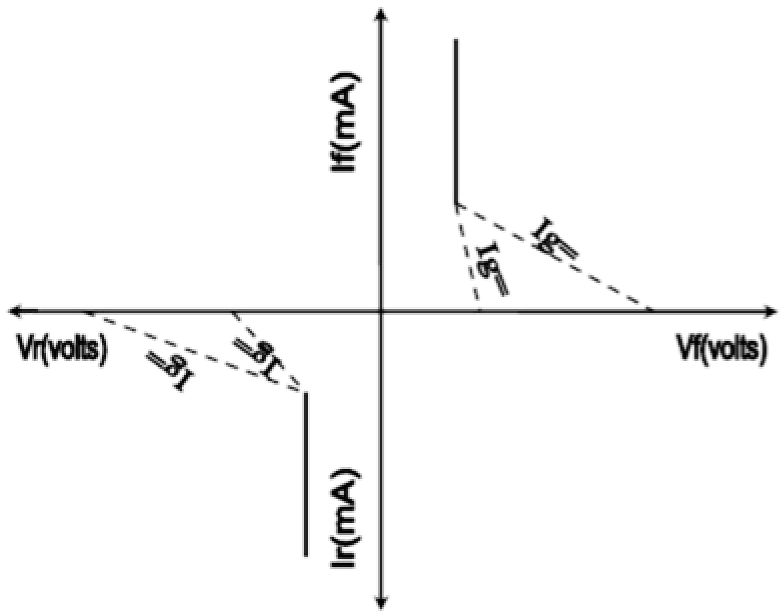


Reverse Direction:

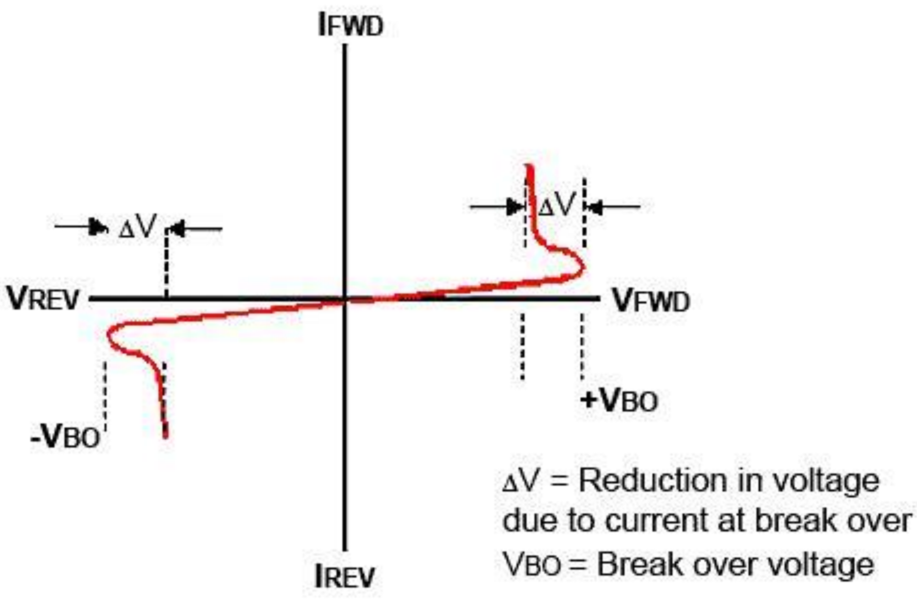


MODEL GRAPH:

TRIAC



DIAC



PROCEDURE:

TRIAC

1. The connections are made as per in the circuit diagram.
2. First by varying RPS 2 then gate current (IG) is kept constant.
3. The voltage between anode and cathode is increased in step by step by varying the RPS
4. The corresponding anode current (IA) is noted.
5. The process is repeated for two more constant value of IG, the readings are tabulated.

DIAC

1. The connections are made as shown in the circuit diagram.
2. First DIAC is connected in forward direction
3. The input supply is increased in step by step by varying the RPS
4. The corresponding ammeter and voltmeter readings are noted and tabulated.
5. Then the DIAC is connected in reverse condition.
6. The above process is repeated

Tabulation:

TRIAC

S.NO	VMT1MT2 (V) when Triac is OFF	IG (mA)	VMT1MT2 (V) when Triac is ON	IMT2 (mA)

DIAC

S.NO	Forward direction		Reverse direction	
	Voltage	Current	Voltage	Current

RESULT:

Thus the V-I characteristics of TRIAC & DIAC was obtained and graph was drawn

Exp. No:10

CHARACTERISTICS OF SCR

AIM:

To obtain the V-I characteristics of SCR and find the break over voltage and holding current.

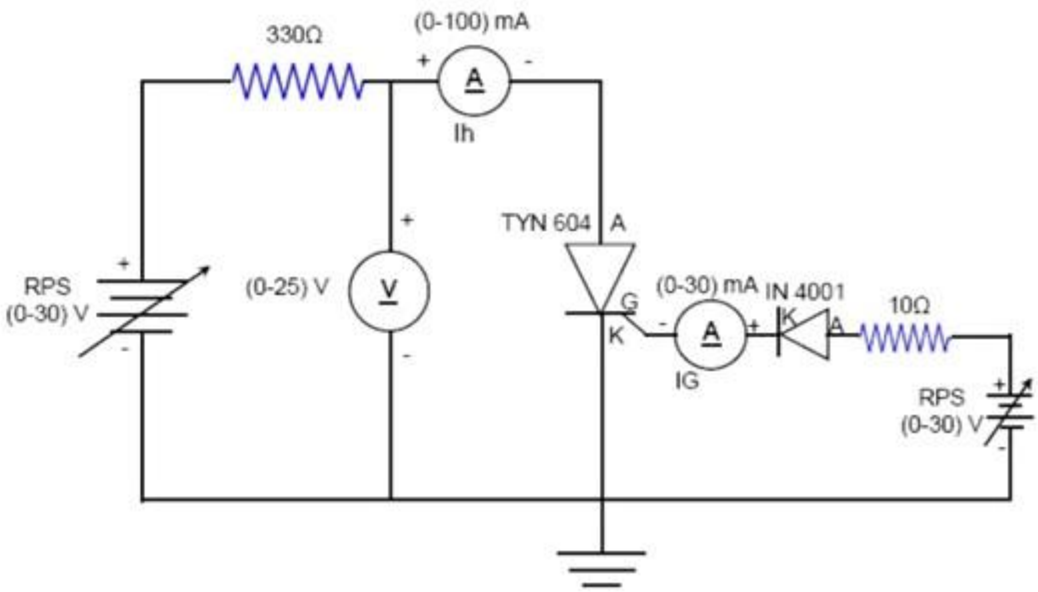
APPARATUS REQUIRED:

S. No.	Name	Range	Qty
1	SCR	TYN604	1
2	Diode	IN4001	1
3	Resistor	330Ω	1
4	Ammeter	(0-50)mA	1
5	Voltmeter	(0-10)V	1
6	RPS	(0-30)V	2
7	Breadboard		1
8	Connecting wires		As required

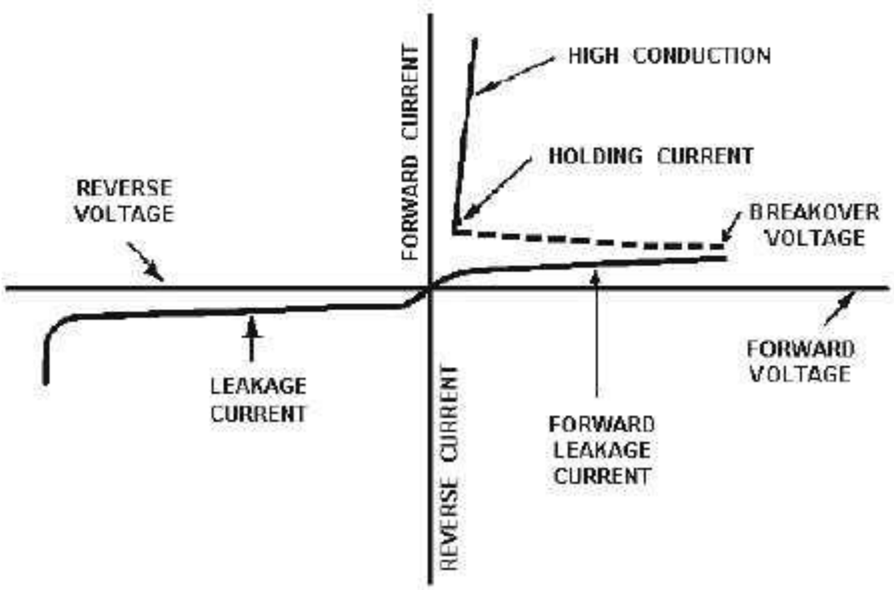
THEORY:

A silicon controlled rectifier (SCR) is a semiconductor device that acts as a true electronic switch. It can change the alternating current in to direct current. It can control the amount of power fed to the load. Thus the SCR combines the features of rectifier and a transistor. If the supply voltage is less than the break over voltage, the gate will open (IG = 0). Then increase the supply voltage from zero, a point is reached when the SCR starts conducting. Under this condition, the voltage across the SCR suddenly drop and most of the supply voltage appears across the load resistance RL. If proper gate current is made to flow the SCR can close at much smaller supply voltage.

CIRCUIT DIAGRAM



MODEL GRAPH:



PROCEDURE:

1. The connections are made as per in the circuit diagram.
2. First by varying RPS 2 then gate current (IG) is kept constant.
3. The voltage between anode and cathode is increased in step by step by varying the RPS .
4. The corresponding anode current (IA) is noted.
5. The process is repeated for two more constant value of IG, the readings are tabulated.

Tabulation:

S.NO	Anode- Cathode voltage	Gate Current	Anode current	Anode- Cathode voltage when SCR is ON

RESULT:

Thus the V-I characteristics of SCR was obtained and graph was drawn