Experiment No: 1

P-N JUNCTION DIODE CHARACTERISTICS

AIM:

1. To plot Volt-Ampere Characteristics of Silicon P-N Junction Diode.
2. To find cut-in Voltage for Silicon P-N Junction diode.
3. To find static and dynamic resistances in both forward and reverse biased conditions for Si P-N Junction diode.

Components:

Name	Qty
Diodes IN 4007(Si)	1
Resistor 1KΩ, 10KΩ	1

Equipment:

Name	Range	Qty
Bread Board	-	1
Regulated Power Supply	0-30V DC	1
Digital Ammeter	0-200μA/20mA	1
Digital Voltmeter	0-2V/20V DC	1
Connecting Wires		

Theory:

Donor impurities (pentavalent) are introduced into one-side and acceptor impurities into the other side of a single crystal of an intrinsic semiconductor to form a p-n diode with a Junction called depletion region (this region is depleted off the charge carriers). This Region gives rise to a potential barrier Vγ called ***Cut- in Voltage***. This is the voltage across the diode at which it starts conducting. It can conduct beyond this Potential.

The P-N junction supports uni-directional current flow. If +ve terminal of the input supply is connected to anode (P-side) and –ve terminal of the input supply is connected to cathode (N- side) then diode is said to be forward biased. In this condition the height of the potential barrier at the junction is lowered by an amount equal to given forward biasing voltage. Both the holes from p-side and electrons from n-side cross the junction simultaneously and constitute a forward current (***injected minority current*** – due to holes crossing the junction and entering N-side of the diode, due to electrons crossing the junction and entering P-side of the diode). Assuming current flowing through the diode to be very large, the diode can be approximated as short-circuited switch.

If –ve terminal of the input supply is connected to anode (p-side) and +ve terminal of the input supply is connected to cathode (n-side) then the diode is said to be reverse biased. In

this condition an amount equal to reverse biasing voltage increases the height of the potential barrier at the junction. Both the holes on p-side and electrons on n-side tend to move away from the junction thereby increasing the depleted region. However the process cannot continue indefinitely, thus a small current called ***reverse saturation current*** continues to flow in the diode. This small current is due to thermally generated carriers. Assuming current flowing through the diode to be negligible, the diode can be approximated as an open circuited switch.

The volt-ampere characteristics of a diode explained by following equation:

$I = I_0 (e^{v/(\eta v_T)} - 1)$ where

I=current flowing in the diode I_0=reverse saturation current

V=voltage applied to the diode

V_T=volt-equivalent of temperature=kT/q=T/11,600=26mV (@ room temp).

η=1 (for Ge) and 2 (for Si)

It is observed that Ge diode has smaller cut-in-voltage when compared to Si diode. The reverse saturation current in Ge diode is larger in magnitude when compared to silicon diode.

Circuit Diagram

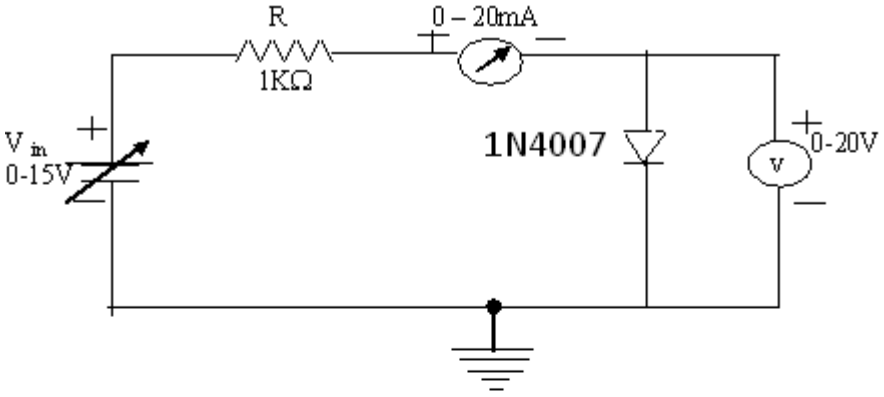
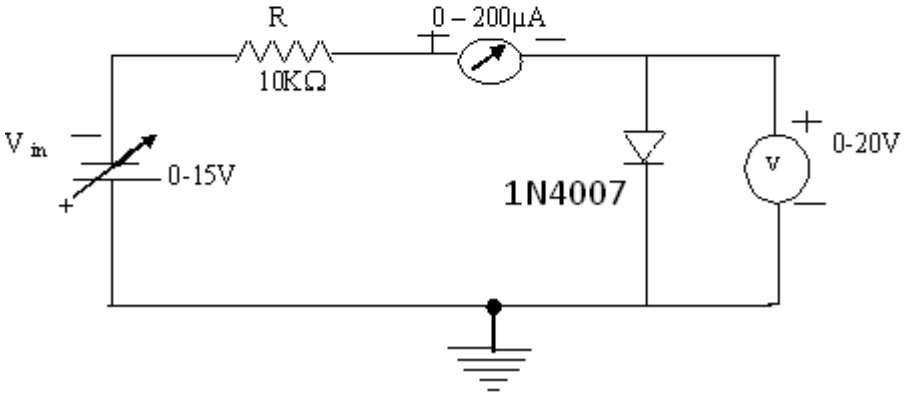


Fig (2) - Reverse Biased condition:



Procedure:

Forward Biased Condition:

1. Connect the circuit as shown in figure (1) using silicon PN Junction diode.
2. Vary V_f gradually in steps of 0.1 volts upto 5volts and note down the corresponding readings of I_f.
3. Step Size is not fixed because of non linear curve and vary the X-axis variable (i.e. if output variation is more, decrease input step size and vice versa).
4. Tabulate different forward currents obtained for different forward voltages.

Reverse biased condition:

1. Connect the circuit as shown in figure (2) using silicon PN Junction diode.
2. Vary V_r gradually in steps of 0.5 volts upto 8 volts and note down the corresponding readings of I_r.
3. Tabulate different reverse currents obtained for different reverse voltages. ($I_r = V_R / R$, where V_R is the Voltage across 10KΩ Resistor).

Observations

Si diode in forward biased conditions:

Sl. No	RPS Voltage	Forward Voltage across the diode V_f (volts)	Forward current through the diode I_f (mA)

Si diode in reverse biased conditions:

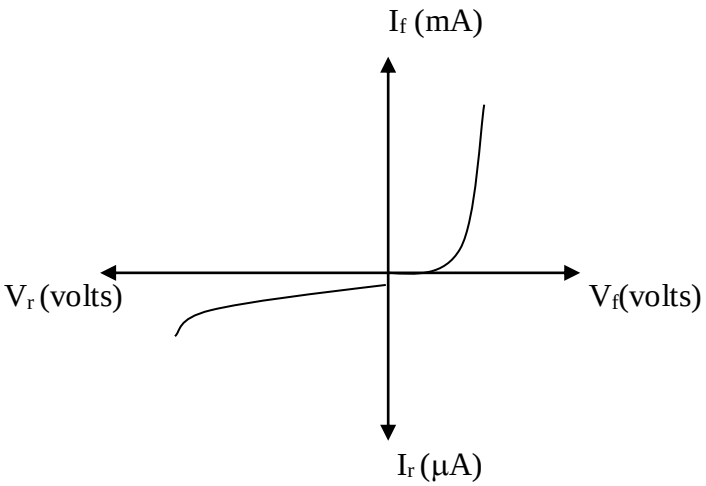
Sl. No	RPS Voltage	Reverse Voltage across the diode V_r (volts)	Reverse current through the diode I_r (μA)

Graph (Instructions):

1. Take a graph sheet and divide it into 4 equal parts. Mark origin at the center of the graph sheet.
2. Now mark + ve x-axis as V_f
   - Ve x-axis as V_r
   + Ve y-axis as I_f
   - ve y-axis as I_r.

3. Mark the readings tabulated for Si forward biased condition in first Quadrant and Si reverse biased condition in third Quadrant.

Calculations from Graph:



Static forward Resistance $R_{dc} = V_f / I_f \Omega$
Dynamic forward Resistance $r_{ac} = \Delta V_f / \Delta I_f \Omega$
Static Reverse Resistance $R_{dc} = V_r / I_r \Omega$

Dynamic Reverse Resistance $r_{ac} = \Delta V_r / \Delta I_r \ \Omega$

Precautions:

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the circuit connections as per the circuit diagram.

Result:

1. Cut in voltage = …… V
2. Static forward resistance = ……. Ω
3. Dynamic forward resistance = ……. Ω

VIVA-VOCEQuestions

1. How depletion region is formed in the PN junction?
2. What are trivalent and pentavalent impurities?
3. What is cut-in or knee voltage? Specify its value in case of Ge or Si?
4. What is maximum forward current and maximum reverse voltage? What is it required?
5. What is leakage current?
6. How does PN-junction diode acts as a switch?
7. What is the effect of temperature in the diode reverse characteristics?
8. What is break down voltage?
9. What is incremental resistance of a diode?
10. What is diode equation?
11. What is the value of V_T in the diode equation?
12. Explain the dynamic resistance of a diode?
13. Explain the phenomenon of breakdown in PN- diode?
14. What is an ideal diode? How does it differ from a real diode?
15. What are the specifications of a diode?
16. Temperature co-efficient of resistance of
    (i) Metals (ii) Intrinsic semiconductor (iii) Extrinsic semiconductor
    (iv) FET (v) BJT
17. What is the internal impedance of
    (i) Ideal current source (ii) Ideal voltage source (iii) Ammeter

Specifications:

For Silicon Diode IN 4007: -

Max. Forward Current	= 1A
Max. Reverse Current	= 30μA
Max. Forward Voltage	= 0.8V
Max. Reverse Voltage	= 1000V
Max. Power dissipation	= 30mw
Temperature	= - 65 to 200^0C

Experiment No: 2

COMMON EMITTER CONFIGURATION

AIM: To study the input and output characteristics of a transistor
In common emitter configuration.

Components:

Name	Qty
Transistor CL 100S	1
Resistor 220KΩ	1
Resistor 560Ω	1

Equipment:

Name	Range	Qty
Bread Board	-	1
Regulated Power Supply	0-30V DC	2
Digital Ammeter	0-20mA /0-200μA	1
Digital Voltmeter	0-2V/20V DC	1
Connecting Wires		

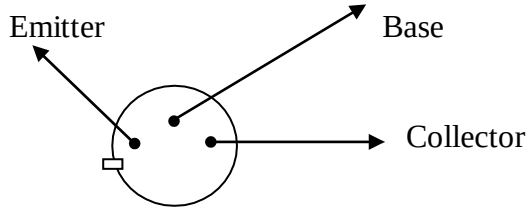
Specifications:

For Transistor **CL 100S**: -

Max. Collector Current = 0.1A

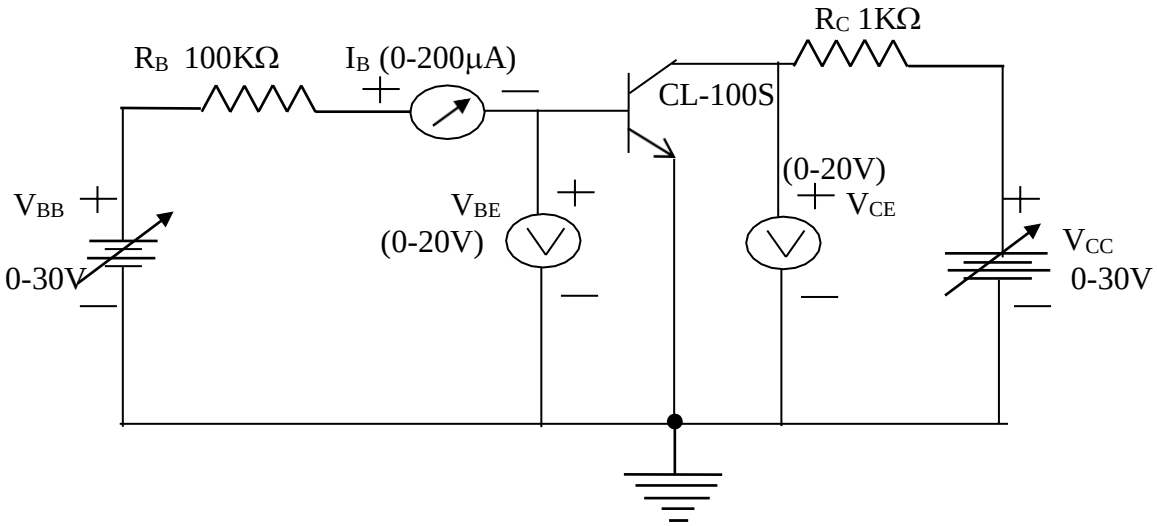
$V_{CEO\ max}$ = 50V

Pin assignment of Transistor:

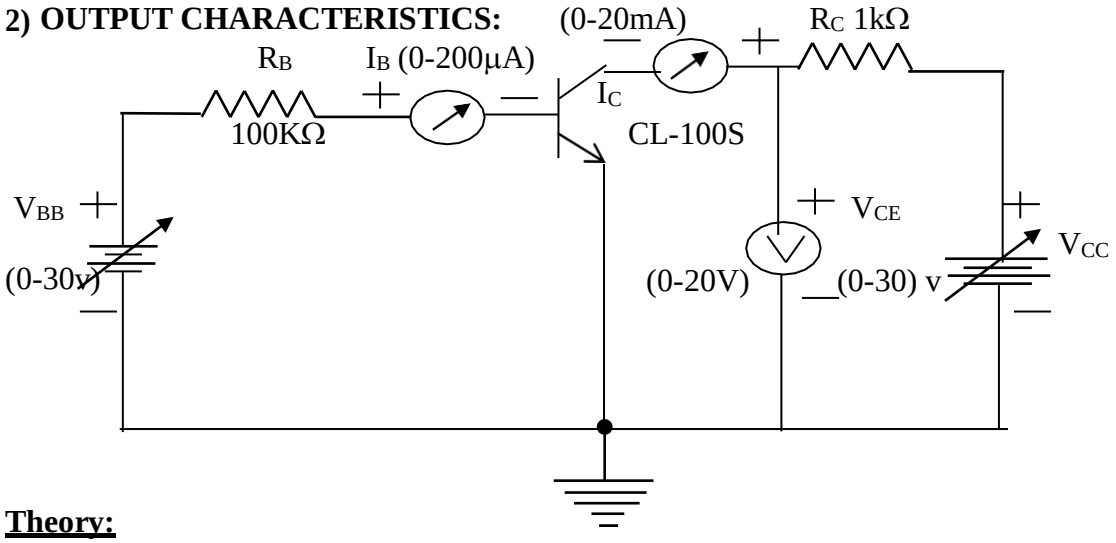


Circuit Diagram:

1) INPUT CHARACTERISTICS



2) OUTPUT CHARACTERISTICS:



Theory:

The basic circuit diagram for studying input and output characteristics are shown in fig (1) & fig (2). In this the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between V_{BE} and I_B at constant V_{CE} in CE configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between V_{CE} and I_C at constant I_B in CE configuration.

Procedure:

Input Characteristics

4. Make the connections as per circuit diagram fig (1).

5. Keep output voltage V_{CE} = 0V by varying V_{CC}.
6. Varying V_{BB} gradually, note down both base current I_B and base - emitter voltage (V_{BE}).

4. Repeat above procedure (step 3) for V_{CE} =5V.

Output Characteristics

5. Make the connections as per circuit diagram fig (2).
6. By varying V_{BB} keep the base current I_B = 20μA.
7. Varying V_{CC} gradually, note down the readings of collector-current (I_C) and collector-emitter voltage (V_{CE}).
8. Repeat above procedure (step 3) for I_E=40μA.

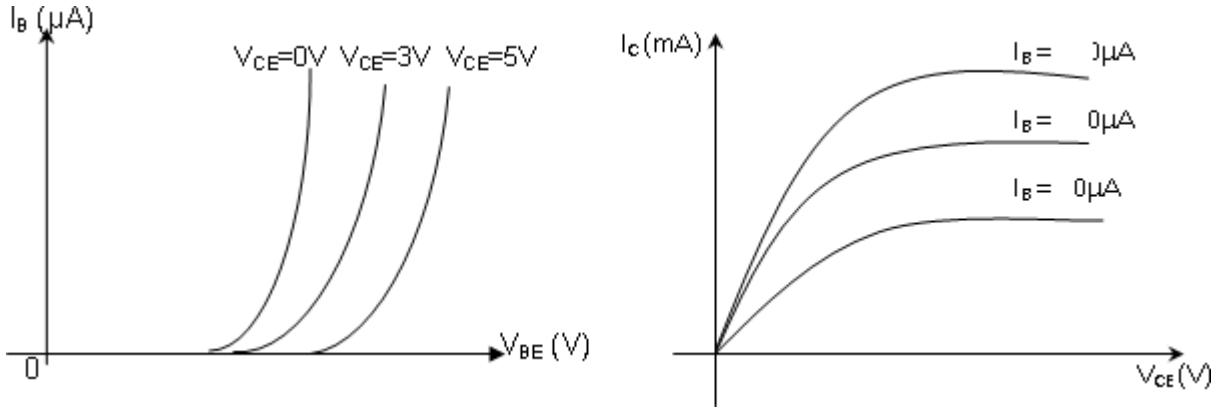
Observations:

I V_{CE} = 0 V		V_{CE} = 5 V	
I_B (μA)	V_{BE} (V)	I_B (μA)	V_{BE} (V)

I_B= 20μA		I_B = 40μA	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)

Input Characteristics **Output Characteristics**

Expected graph:



3. Plot Input Characteristics and output Characteristics: the input characteristics by taking V_{BE} on Y-axis and I_B on X-axis at constant V_{CE}.
4. Plot the output characteristics by taking V_{CE} on Y-axis and I_C on X-axis by taking I_B as a parameter.

Calculations from graph:

2. **Input resistance:** To obtain input resistance find ΔV_{BE} and ΔI_B at constant V_{CE} on one of the input characteristics.
   Then $R_i = \Delta V_{BE} / \Delta I_B$ (V_{CE} constant)

2. **Output resistance:** To obtain output resistance, find ΔI_C and ΔV_{CE} at Constant I_B.

   $R_o = \Delta V_{CE} / \Delta I_C$ (I_B constant)

Inference:

1. Medium Input and Output resistances.
2. Smaller value of V_{CE} comes earlier cut-in-voltage.
3. Increase in the value of I_B causes saturation of the transistor at an Earlier voltage.

Precautions:

4. While doing the experiment do not exceed the ratings of the Transistor. This may lead to damage the transistor.
5. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
6. Do not switch **ON** the power supply unless you have checked the Circuit connections as per the circuit diagram.
7. Make sure while selecting the emitter, base and collector terminals of the transistor.

Result:

1. Input Resistance (R_i) = ... Ω

2. Output Resistance (R_o) = ...Ω

3. $\beta = Ic/I_B$ |vce=constant _____

Viva-VoceQuestions

1. Two discrete diodes connected back-to-back cannot work as a transistor, why?
2. For amplification, CE configuration is preferred, why?
3. To operate a transistor as amplifier, the emitter junction is forward biased and thecollector junction is reversed biased, why?
4. With the rise in temperature, the leakage collector current increases, why?
5. An electronic device transistor is named as transistor, why?
6. Most of the transistor are ***NPN*** type and not ***PnP***, why?
7. The forward resistance of emitter junction is slightly less than forward resistance ofcollector junction, why?

Experiment No: 2

COMMON EMITTER CONFIGURATION

AIM: To study the input and output characteristics of a transistor
In common emitter configuration.

Components:

Name	Qty
Transistor CL 100S	1
Resistor 220KΩ	1
Resistor 560Ω	1

Equipment:

Name	Range	Qty
Bread Board	-	1
Regulated Power Supply	0-30V DC	2
Digital Ammeter	0-20mA /0-200μA	1
Digital Voltmeter	0-2V/20V DC	1
Connecting Wires		

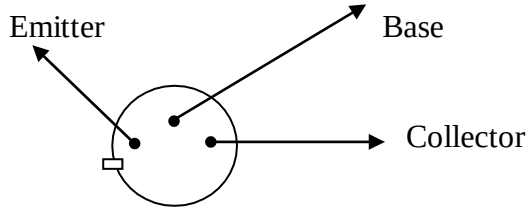
Specifications:

For Transistor **CL 100S**: -

Max. Collector Current = 0.1A

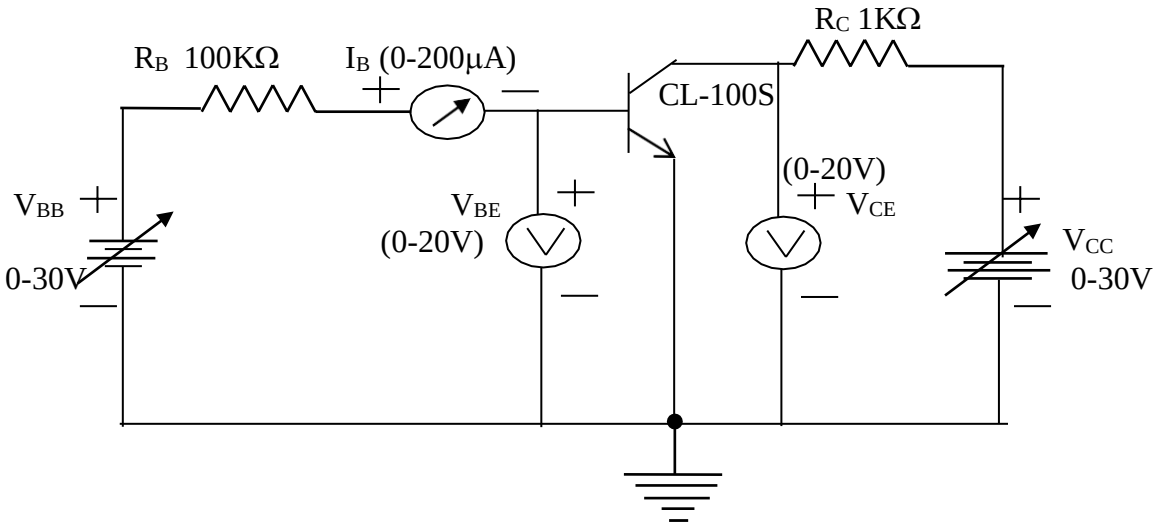
$V_{CEO\ max}$ = 50V

Pin assignment of Transistor:

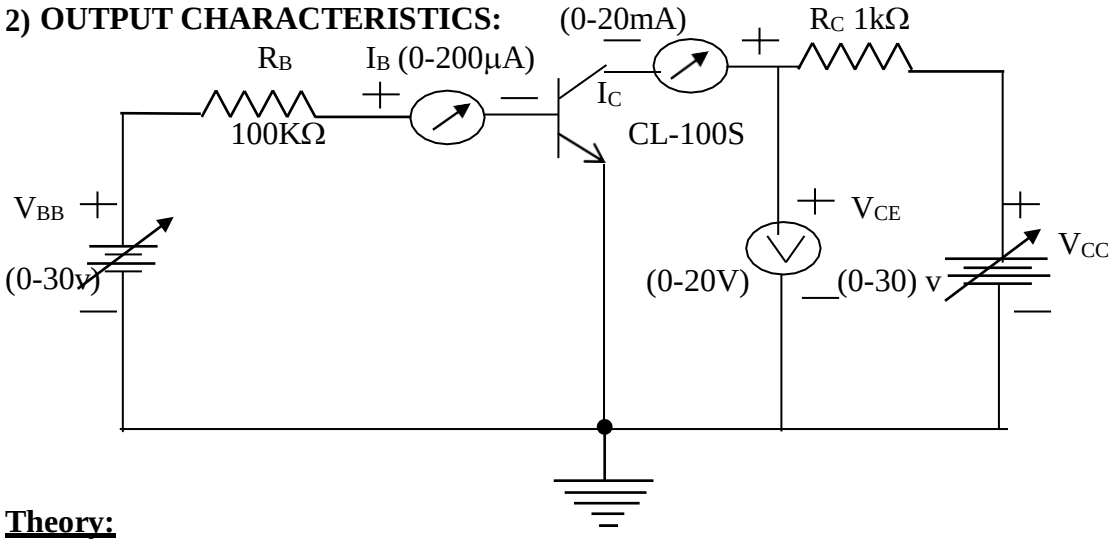


Circuit Diagram:

1) INPUT CHARACTERISTICS



2) OUTPUT CHARACTERISTICS:



Theory:

The basic circuit diagram for studying input and output characteristics are shown in fig (1) & fig (2). In this the input is applied between base and emitter and the output is taken from collector and emitter. Here emitter is common to both input and output and hence the name common emitter configuration.

Input characteristics are obtained between the input current and input voltage taking output voltage as parameter. It is plotted between V_{BE} and I_B at constant V_{CE} in CE configuration.

Output characteristics are obtained between the output voltage and output current taking input current as parameter. It is plotted between V_{CE} and I_C at constant I_B in CE configuration.

Procedure:

Input Characteristics

4. Make the connections as per circuit diagram fig (1).

5. Keep output voltage V_{CE} = 0V by varying V_{CC}.
6. Varying V_{BB} gradually, note down both base current I_B and base - emitter voltage (V_{BE}).

4. Repeat above procedure (step 3) for V_{CE} =5V.

Output Characteristics

5. Make the connections as per circuit diagram fig (2).
6. By varying V_{BB} keep the base current I_B = 20μA.
7. Varying V_{CC} gradually, note down the readings of collector-current (I_C) and collector-emitter voltage (V_{CE}).
8. Repeat above procedure (step 3) for I_E=40μA.

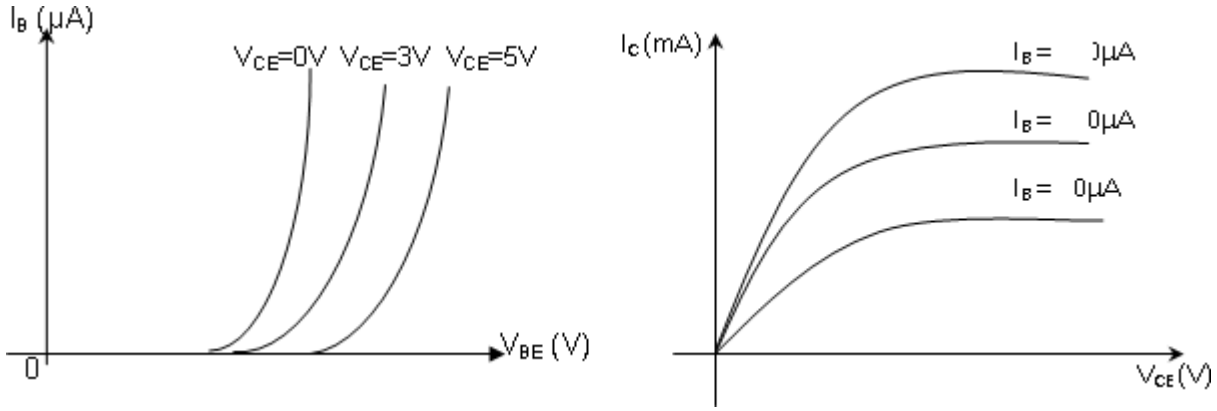
Observations:

I V_{CE} = 0 V		V_{CE} = 5 V	
I_B (μA)	V_{BE} (V)	I_B (μA)	V_{BE} (V)

I_B= 20μA		I_B = 40μA	
V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)

Input Characteristics **Output Characteristics**

Expected graph:



3. Plot Input Characteristics and output Characteristics: the input characteristics by taking V_{BE} on Y-axis and I_B on X-axis at constant V_{CE}.
4. Plot the output characteristics by taking V_{CE} on Y-axis and I_C on X-axis by taking I_B as a parameter.

Calculations from graph:

2. **Input resistance:** To obtain input resistance find ΔV_{BE} and ΔI_B at constant V_{CE} on one of the input characteristics.
   Then $R_i = \Delta V_{BE} / \Delta I_B$ (V_{CE} constant)

2. **Output resistance:** To obtain output resistance, find ΔI_C and ΔV_{CE} at Constant I_B.

   $R_o = \Delta V_{CE} / \Delta I_C$ (I_B constant)

Inference:

1. Medium Input and Output resistances.
2. Smaller value of V_{CE} comes earlier cut-in-voltage.
3. Increase in the value of I_B causes saturation of the transistor at an Earlier voltage.

Precautions:

4. While doing the experiment do not exceed the ratings of the Transistor. This may lead to damage the transistor.
5. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
6. Do not switch **ON** the power supply unless you have checked the Circuit connections as per the circuit diagram.
7. Make sure while selecting the emitter, base and collector terminals of the transistor.

Result:

1. Input Resistance (R_i) = ... Ω

2. Output Resistance (R_o) = ...Ω

3. $\beta = Ic/I_B$ |vce=constant _____

Viva-VoceQuestions

1. Two discrete diodes connected back-to-back cannot work as a transistor, why?
2. For amplification, CE configuration is preferred, why?
3. To operate a transistor as amplifier, the emitter junction is forward biased and thecollector junction is reversed biased, why?
4. With the rise in temperature, the leakage collector current increases, why?
5. An electronic device transistor is named as transistor, why?
6. Most of the transistor are ***NPN*** type and not ***PnP***, why?
7. The forward resistance of emitter junction is slightly less than forward resistance ofcollector junction, why?

Experiment No: 3

FET CHARACTERISTICS

AIM: To study Drain Characteristics and Transfer Characteristics of a FET.

Components:

Name	Qty
JFET BFW 10	1
Resistors 470Ω	2

Equipment:

Name	Range	Qty
FET Trainer Kit	-	1
Digital Ammeter	0-20mA	1
Digital Voltmeter	0-20 V	2
Connecting Wires		

Specifications:

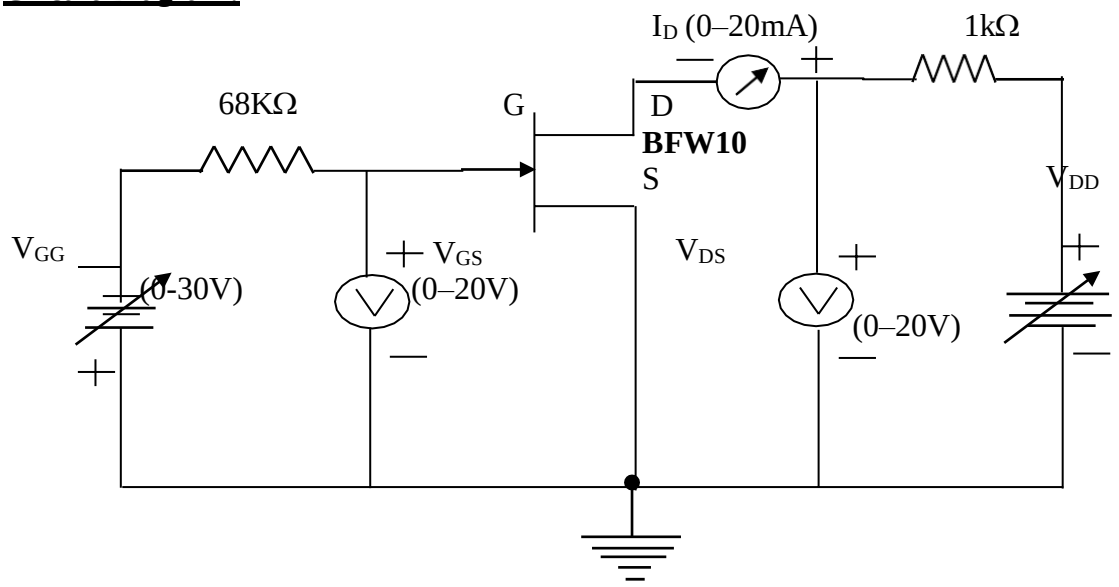
For **JFET BFW10**: -

Gate Source Voltage VGS = - 30V

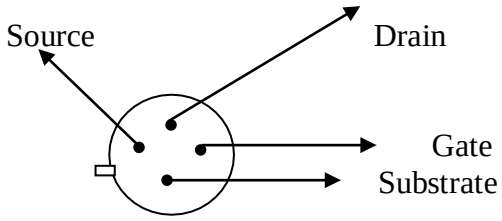
Forward Gain Current I_{GF} = 10 mA

Maximum Power Dissipation P_D = 300 mW.

Circuit Diagram:



Pin assignment of FET:



Theory:

The basic circuit diagram for studying drain and transfer characteristics is Shown in figure.

Drain characteristics are obtained between the drain to source voltage (V_{DS}) and drain current (I_D) taking gate to source voltage (V_{GS}) as the parameter.

Transfer characteristics are obtained between the gate to source voltage (V_{GS}) and Drain current (I_D) taking drain to source voltage (V_{DS}) as parameter.

Procedure:

DRAIN CHARACTERISTICS

1. Make the connections as per circuit diagram.
2. Keep V_{GS} = 0V by varying V_{GG}.
3. Varying V_{DD} gradually, note down both drain current I_D and drain to source voltage (V_{DS}).
4. Repeat above procedure (step 3) for V_{GS} = -1V.

TRANSFER CHARACTERISTICS:

1. Keep V_{DS} = 2V by varying V_{DD}.
2. Varying V_{GG} gradually from 0 – 5V, note down both drain current (I_D) and gate to source voltage (V_{GS}).
3. Repeat above procedure (step 2) for V_{DS} = 4V.

Observations:

DRAIN CHARACTERISTICS:

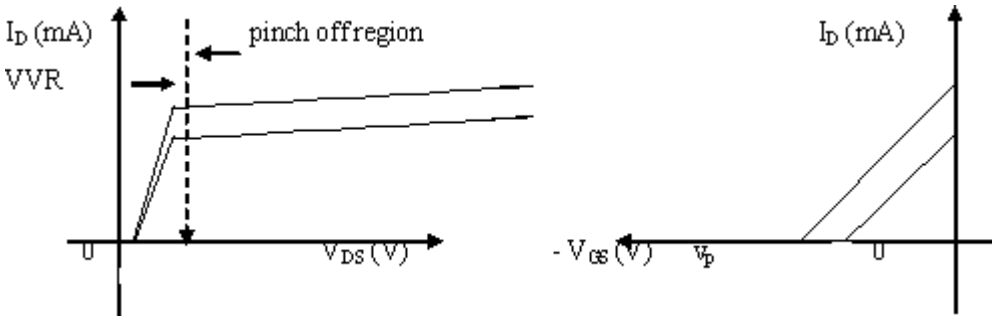
V_{GS} = 0V		**V_{GS} = -1V**	
V_{DS} (V)	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**

TRANSFER CHARACTERISTICS:

V_{DS} = 2V		V_{DS} = 4V	
V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

Graph (Instructions):

1. Plot the drain characteristics by taking V_{DS} on X-axis and I_D on Y-axis at constant V_{GS}.
2. Plot the Transfer characteristics by taking V_{GS} on X-axis and I_D on Y-axis at constant V_{DS}.



DRA

IN CHARACTERISTICS **TRANSFER CHARACTERISTICS**

Calculations from Graph:

Drain Resistance (r_d) **:** It is given by the ration of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain current (ΔI_D) for a constant gate to source voltage (V_{GS}), when the JFET is operating in pinch-off or saturation region.

Trans-Conductance (g_m) **:** Ratio of small change in drain current (ΔI_D) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant V_{DS}.

$g_m = \Delta I_D / \Delta V_{GS}$ at constant V_{DS}. (From transfer characteristics)

The value of g_m is expressed in mho's ( ) or siemens (s).

Amplification Factor (μ) **:** It is given by the ratio of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in gate to source voltage (ΔV_{GS}) for a constant drain current.

$\mu = \Delta V_{DS} / \Delta V_{GS.}$

$$\mu = (\Delta V_{DS} / \Delta I_D) \text{ X } (\Delta I_D / \Delta V_{GS})$$

$$\mu = r_d \text{ X } g_m.$$

Inference:

1. As the gate to source voltage (V_{GS}) is increased above zero, pinch off voltage is increased at a smaller value of drain current as compared to that when V_{GS} =0 V
2. The value of drain to source voltage (V_{DS}) is decreased as compared to that when V_{GS} =0 V

Precautions:

1. While doing the experiment do not exceed the ratings of the FET. This may lead to damage the FET.
2. Connect voltmeter and Ammeter in correct polarities as shown in the Circuit diagram.
3. Do not switch **ON** the power supply unless you have checked the Circuit connections as per the circuit diagram.
4. Make sure while selecting the Source, Drain and Gate terminals Of the FET.

Result:

1. Drain Resistance (r_d) = …….
2. Transconductance (g_m) = …….
3. Amplification factor (μ) = ……

Viva voce Questions

1. Why FET is called as a unipolar transistor?
2. What are the advantages of FET?
3. What is the difference between MOSFET and FET?
4. What is Trans conductance?
5. What is amplification factor?
6. Why thermal runaway does not occur in FET?

7. State weather FET is voltage controlled or current controlled and also state the reason?
8. State why BJT is current controlled device?
9. Why current gain is important parameter in BJT where as conductance is important Parameter in FET?
10. Why we plot input and output characteristics? What information we can obtain?

Experiment No: 4

HALF WAVE RECTIFIER WITH & WITHOUT FILTERS

AIM: Study of Half – wave rectifier with & without Filter and to finds Ripple Factor.

EQUIPMENT:

Name	Range	Quantity
Transformer	9-0-9V/12-0-12V	1
Bread Board		1
Digital Multimeter		1
Resistor	1kΩ,10kΩ	1
Connecting wires		

THEORY:

The conversion of AC into DC is called Rectification. Electronic devices can convert AC power into DC power with high efficiency

Consider the given circuit. Assume the diode to be ideal i.e. $V_f = 0$, $R_r = \infty$, $R_s = 0$. During the positive half cycle, the diode is forward biased and it conducts and hence a current flows through the load resistor. During the negative half cycle, the diode is reverse biased and it is equivalent to an open circuit, hence the current through the load resistance is zero. Thus the diode conducts only for one half cycle and results in a half wave rectified output.

MATHEMATICAL ANALYSIS

(Neglecting R_f and R_s)

Let $V_{ac} = V_m \sin\omega t$ is the input AC signal, the current I_{ac} flows only for one half cycle i.e. from $\omega t = 0$ to $\omega t = \pi$, where as it is zero for the duration

$\pi \leq \omega T \leq 2\pi$

Therefore, $I_{ac} = V_{ac}/R = V_m \text{ Sinwt}/R$

$$= I_m \sin\omega t \quad 0 \leq \omega t \leq \pi$$

$$= 0 \quad \pi \leq \omega t \leq 2\pi$$

Where I_m = maximum value of current
V_m = maximum value of voltage

AVERAGE OR DC VALUE OF CURRENT

$$I_{dc} = 1/2\pi \int_0^{2\pi} I_m (\sin\omega t)\, d\omega t$$

$$I_{dc} = 1/2\pi \left[\int_0^{\pi} \sin\omega t \, d\omega t + \int_{\pi}^{2\pi} 0 \, d\omega t \right] = Im / \pi$$

Similarly

$V_{dc} = V_m / \pi$

The RMS VALUE OF CURRENT

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_{ac}^2 \, d\omega t}$$

$$= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_m^2 \sin^2 d\omega t}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \frac{1-\cos 2\omega t}{2} \, d\omega t} = \frac{I_m}{2}$$

Similarly

RIPPLE FACTOR:

$$V_{rms} = \frac{V_m}{2}$$

The output of a half – wave rectifier consists of some undesirable ac components known as ripple. These can be removed using suitable filter circuits.

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol

$$\gamma = \frac{V_{ac}}{V_{dc}}$$

$$V^2_{rms} = V^2_{ac} + V^2_{dc}$$

$$\gamma = \frac{\sqrt{V^2_{rms} - V^2_{dc}}}{V_{dc}}$$

Converting V_{rms} and V_{dc} into its corresponding V_m value, we get

$\gamma = 1.21$

RECTIFICATION FACTOR:

The ratio of output DC power to the input AC power is defined as efficiency

Output power = $I^2_{dc}R$
Input power = $I^2_{rms}(R+R_f)$

Where R_f – forward resistance of the diode

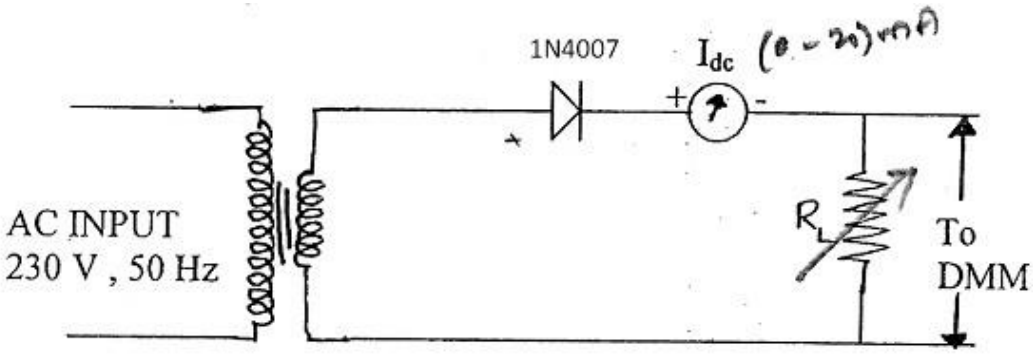
$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I^2_{dc}R}{I^2_{rms}(R+R_f)}$$

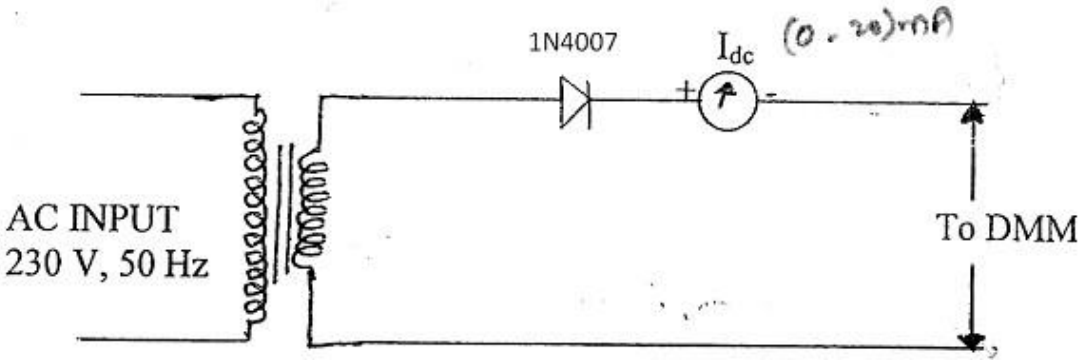
$$\eta = \frac{4}{\pi^2} \times \frac{R}{R + R_f}$$

= 40.5 % (if $R_f << R$, R_f can be neglected).

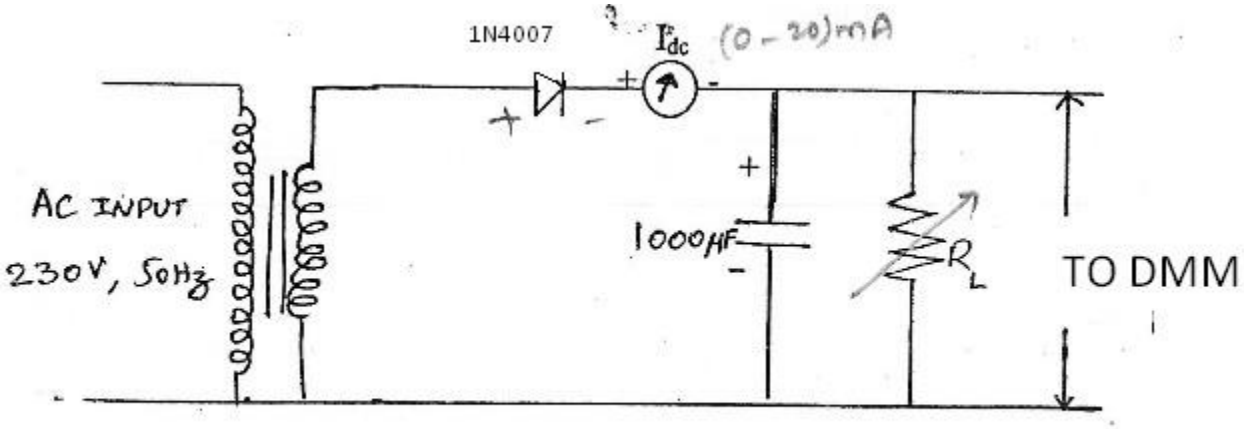
CIRCUIT DIAGRAM:

Half Wave Rectifier (with out filter):





Half Wave Rectifier (with C-filter):



PROCEDURE:

1. Make connections as per the Circuit Diagram.
2. Note down the AC and DC Voltages and Currents without Filter and with Load.
3. And again observe the AC and DC Voltages and Currents with L & Π Filters and with load.
4. Observe the Voltage across the secondary of the Transformer.

Tabular Column:

V_{ac} =_____(Voltage across the secondary of the transformer)

Condition	**V_{ac}**	**V_{dc}**	**V_m**	**R**
Without Filter				

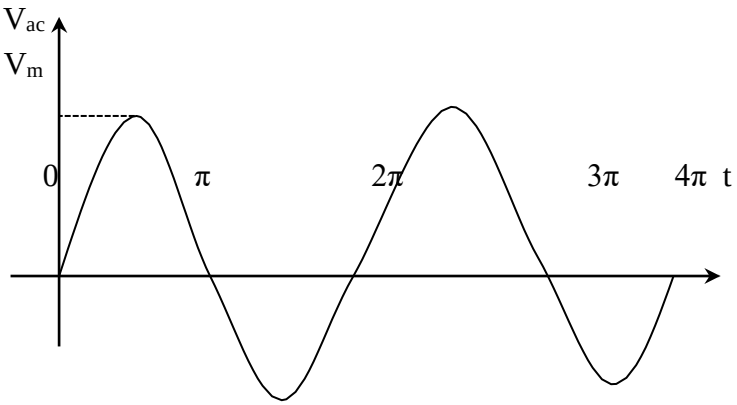
Condition	**V_{ac}**	**V_{dc}**	**V_m**	**C**	**R**
With C Filter					

CALCULATIONS:

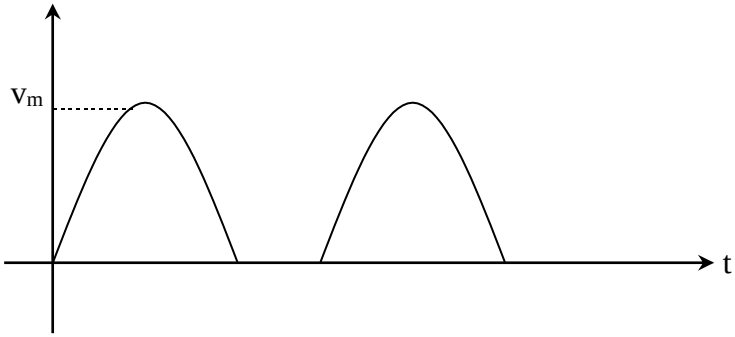
$$\text{Ripple factor} \quad \gamma = \frac{V_{ac}}{V_{dc}}$$

EXPECTED WAVEFORMS:

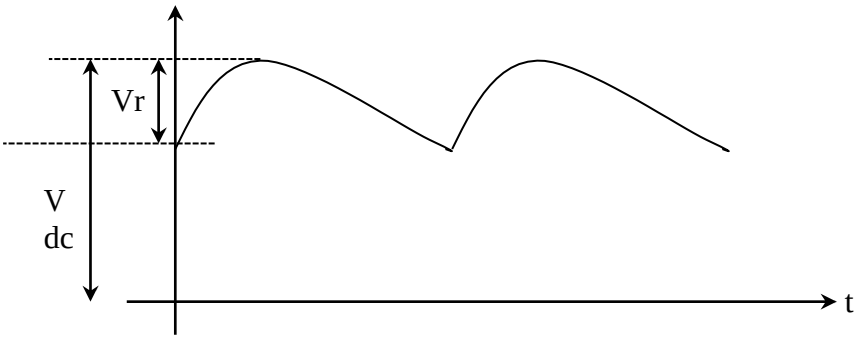
Input Waveform



HWR WITHOUT FILTER:



HWR WITH FILTER:



V_R = Ripple Voltage

RESULT: -

Parameters	Without filter	With c - Filter
Ripple Factor		
Efficiency		

VIVA-VOCE Questions

1. Why are rectifiers used with a filter at their output?
2. What is the voltage regulation of the rectifier?
3. What is the ideal value of regulation?
4. What does no load condition refer to?
5. What are the advantages of bridge rectifier?
6. What are the advantages and disadvantages of capacitor filter?
7. What are the applications of rectifiers?
8. What is the regulation for a
   (i) Half - wave circuit (ii) Full-wave circuit
9. What is PIV? State it value in case of (i) Half wave (ii) Full wave (iii) Bridge rectifier.
10. What is the output signal frequency in case of (i) Half wave (ii) Full wave (iii) Bridge rectifier?

FULLWAVE RECTIFIER WITH & WITHOUT FILTERS

AIM: To Study the Full – wave rectifier Circuit & to Find its, Ripple factor

EQUIPMENT:

Name	Range	Quantity
Transformer	9-0-9V/12-0-12V	1
Bread Board		1
Digital Multimeter		1
Resistor	1kΩ,10kΩ	1
Connecting wires		

THEORY:

The conversion of AC into DC is called Rectification. Electronic devices can convert AC power into DC power with high efficiency

FULL-WAVE RECTIFIER:

The full-wave rectifier consists of a center-tap transformer, which results in equal voltages above and below the center-tap. During the positive half cycle, a positive voltage appears at the anode of D_1 while a negative voltage appears at the anode of D_2. Due to this diode D_1 is forward biased it results in a current I_{d1} through the load R.

During the negative half cycle, a positive voltage appears at the anode of D_2 and hence it is forward biased. Resulting in a current I_{d2} through the load at the same instant a negative voltage appears at the anode of D_1 thus reverse biasing it and hence it doesn't conduct.

MATHEMATICAL ANALYSIS (Neglecting R_f and R_s)

The current through the load during both half cycles is in the same direction and hence it is the sum of the individual currents and is unidirectional

Therefore, $I = I_{d1} + I_{d2}$

$$V_{ac} = V_m \sin \omega t$$

$$I_{d1} = \frac{V_m}{R}\sin\omega t \qquad 0 \le \omega t \le \pi$$
$$= 0 \qquad \pi \le \omega t \le 2\pi$$

$$I_{d2} = 0 \qquad 0 \le \omega t \le \pi$$
$$= \frac{-V_m}{R}\sin\omega t \qquad \pi \le \omega t \le 2\pi$$

The individual currents and voltages are combined in the load and there fore their average values are double that obtained in a half – wave rectifier circuit.

AVERAGE OR DC VALUE OF CURRENT I_{dc}

$$I_{dc} = 1/2\pi \left[\int_0^{\pi} I_m (\sin\omega t)\, d\omega t - \int_{\pi}^{2\pi} I_m (\sin\omega t)\, d\omega t \right] = 2 I_m / \pi$$

Similarly,

$$V_{dc} = 2V_m / \pi$$

The RMS VALUE OF CURRENT

$$= \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_m^2 \sin^2 \omega t\, d\omega t}$$

$$= \frac{m}{\sqrt{2\pi}}$$

Similarly, $V_{rms} = \frac{V_m}{\sqrt{2\pi}}$

RIPPLE FACTOR

Ripple factor is defined as the ratio of the effective value of AC components to the average DC value. It is denoted by the symbol γ

$$\gamma = \frac{V_{ac}}{V_{dc}}$$

($\gamma = 0.48$)

RECTIFICATION FACTOR

The ratio of output DC power to the input AC power is defined as efficiency

Efficiency, η

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{V_{dc} * I_{dc}}{V_{rms}\sqrt{I_{ac}^{\ 2} + I_{dc}^{\ 2}}} * 100$$

η = 81% (if R >> R_f . then R_f can be neglected)

Where R_f – forward resistance of two diode

Peak – Inverse – Voltage (PIV)

It is the maximum voltage that has to be with stood by a diode when it is reverse biased

$$PIV = 2V_m$$

Advantages of Full wave Rectifier

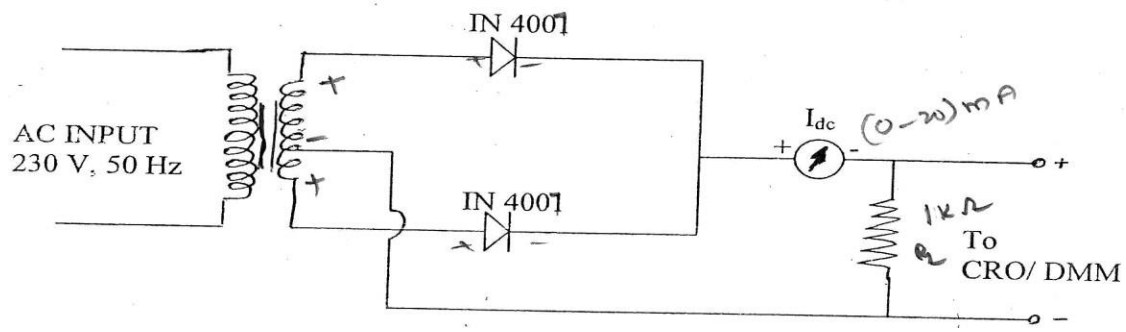
1. γ is reduced
2. η is improved

Disadvantages of Full wave Rectifier

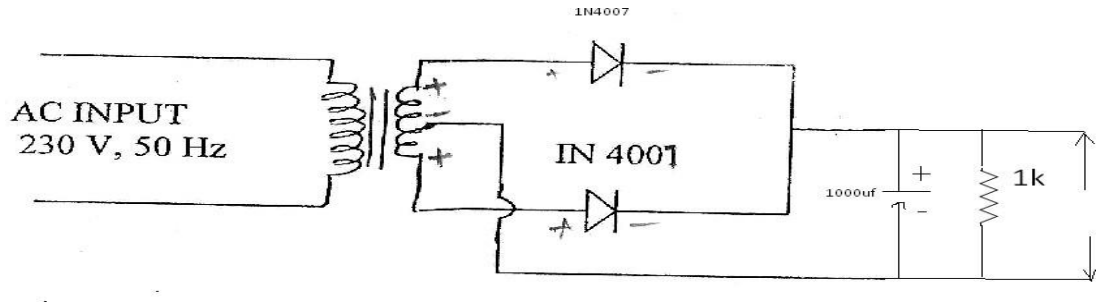
1. Output voltage is half the secondary voltage
2. Diodes with high PIV rating are used

Manufacturing of center-taped transformer is quite expensive and so Full wave rectifier with center-taped transformer is costly.

CIRCUIT DIAGRAM (With out Filter):



(With C -Filter) :



PROCEDURE:

5. Make connections as per the Circuit Diagram.
6. Note down the AC and DC Voltages and Currents without Filter and with Load.
7. And again observe the AC and DC Voltages and Currents with Filter and with load.
8. Observe the Voltage across the secondary of the Transformer (i.e. V_{rms}).

Tabular Column:

Condition	**V_{ac}**	**V_{dc}**	**Vm**	**R**
Without Filter				

Condition	**V_{ac}**	**V_{dc}**	**Vm**	**C**	**R**
With C Filter					

CALCULATIONS:

Ripple factor $\gamma = \dfrac{V_{ac}}{V_{dc}}$

Efficiency $\eta = \dfrac{P_{dc}}{P_{ac}} = \dfrac{V_{dc} * I_{dc}}{V_{rms}\sqrt{I_{ac}^{\,2} + I_{dc}^{\,2}}} * 100$

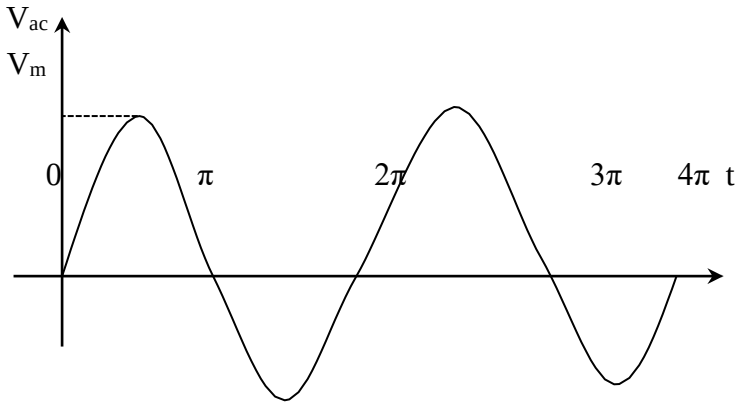
Percentage of regulation $= \dfrac{V_{NL} - V_{FL}}{V_{FL}} X\ 100\ \%$

V_{NL} = Voltage across load resistance,
When minimum current flows though it

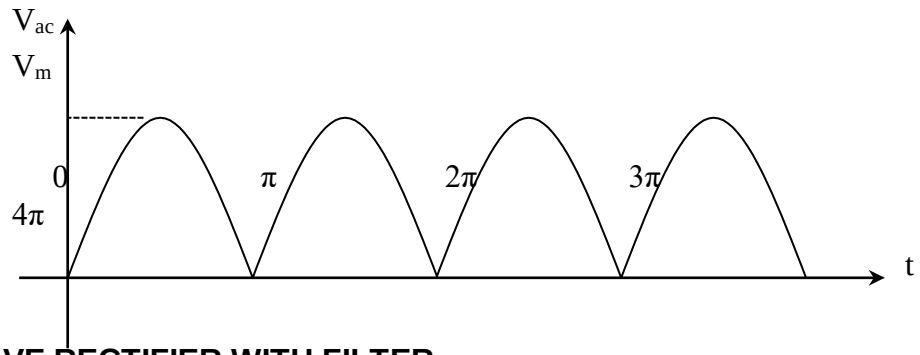
V_{FL} = Voltage across load resistance, When maximum current flows through it.

EXPECTED WAVEFORMS:

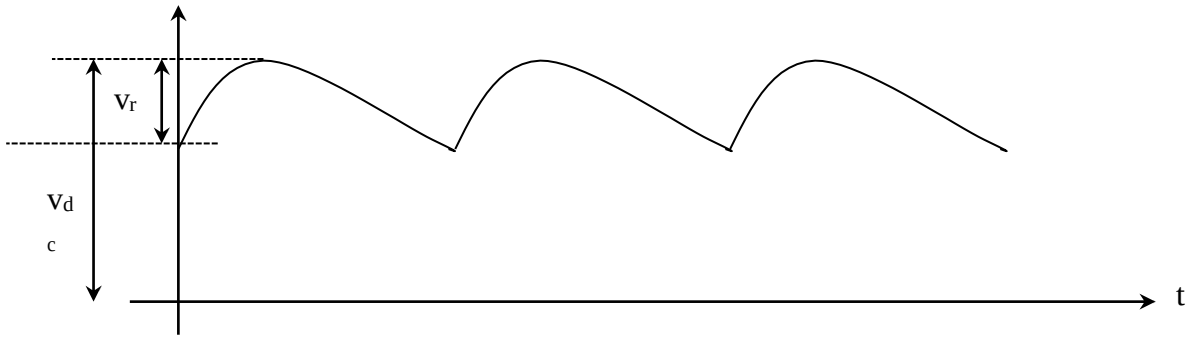
Input Waveform



FULLWAVE RECTIFIER WITHOUT FILTER:



FULLWAVE RECTIFIER WITH FILTER:



V_R = Ripple Voltage

RESULT:

Parameters	Without filter	With C Filter
Ripple Factor		
Efficiency		

VIVA-VOCE Questions

1. A diode should not be employed in the circuits where it is to carry more than its maximum forward current, why?
2. While selecting a diode, the most important consideration is its PIV, why?
3. The rectifier diodes are never operated in the breakdown region, why?
4. In filter circuits, a capacitor is always connected in parallel, why?

   In filter circuits, an inductor is always connected in series why?

Exp. No: 5

SIMULATION AND HARDWARE REALISATION OF CLIPPING AND CLAMPING CIRCUITS

5(a).CLIPPER

AIM:

To construct a Clipper using diode and to draw its performance characteristics.

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1.	Function Gen	-	1
2.	Diode	IN4001	2
3.	Resistor	1KΩ	1
4.	Bread Board	-	1
5.	Capacitor	100μf	1
6.	CRO	-	1

Theory:

Clipper circuits have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half wave rectifier of the previous experiment is an example of the simplest form of diode clipper. Depending on the orientation of thy diode, the positive or negative region of the input signal is "clipped" off. There are two general categories of clippers: series and parallel. The series c configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in branch parallel to the load.

Circuit Diagram:

PRECAUTIONS:

1) The primary and secondary sides of the transformer should be carefully identified.
2) The polarities of the diode should be carefully identified.
3) While determining the % regulation, first Full load should be applied and then it should be decremented in steps.

RESULT:

The Ripple factor and the % regulation for the Full-Wave Rectifier with and without filters are calculated.

1.The Ripple factor of Full-Wave Rectifier without filter is _____

2.The Ripple factor of Full-Wave Rectifier with filter is _____

3.The % Regulation of Full-Wave Rectifier without filter is _____

4.The % Regulation of Full-Wave Rectifier with filter is _____

5(b).CLAMPER

AIM:

To construct a Clamper using diode and to draw its performance characteristics.

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1.	Function Gen	-	1
2.	Diode	IN4001	2
3.	Resistor	1KΩ	1
4.	Bread Board	-	1
5.	Capacitor	100μf	1
6.	CRO	-	1

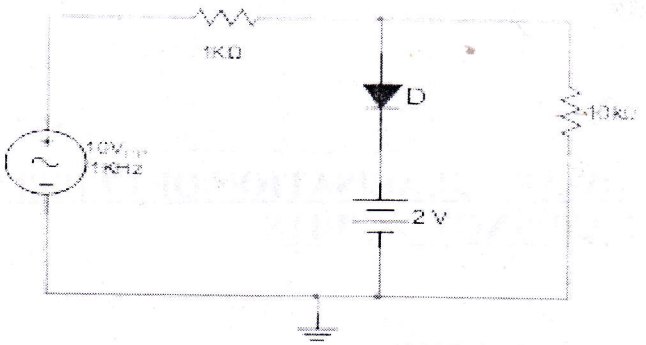
Theory:

Sometimes you may want to leave the waveform unchanged, but modify its DC level up or down. To accomplish this, you use a clamper circuit. The beauty of clampers is that they can adjust the DC position of the waveform without knowing what the waveform actually is. The positive clamper shown in the figure below works as follows:

In the positive half of the first cycle, the voltage across the capacitor cannot change instantaneously; therefore as the voltage on the input moves up, the voltage on the top of the diode has to follow this voltage. This reverse biases the diode causing it to act as an open, thus the output voltage follows the input voltage. As the input voltage drops into the negative half of the first cycle, the diode is going to be forward biased. In the positive half of the first cycle, the voltage across the capacitor cannot change instantaneously; therefore as the voltage on the input moves up, the voltage on the top of the diode has to follow this voltage.

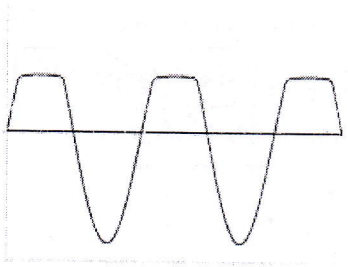
This reverse biases the diode causing it to act as an open, thus the output voltage follows the input voltage. As the input voltage drops into the negative half of the first cycle, the diode is going to be forward biased. This causes the diode to behave like a wire, which cannot dissipate any voltage. This causes to inter-related effects. First, the output voltage is held steady at 0V. Second, because there are 0V dissipated across the diode (and resistor) all of the voltage has to be dissipated across the capacitor. This charges the capacitor to the magnitude of the input signal.

Circuit Diagram:

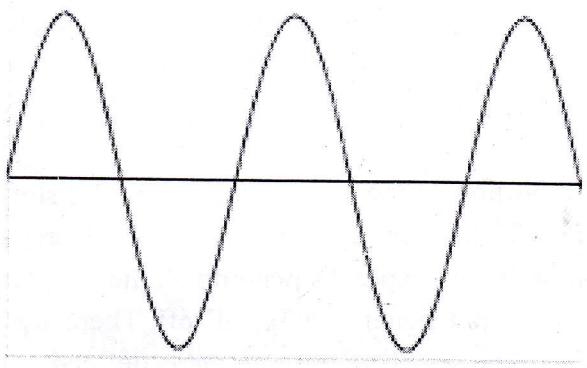


Model Graph:

Input Characteristics:



Output characteristics:



Procedure:

Clipping Circuit:

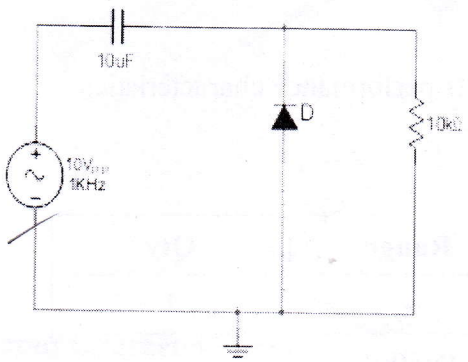
1. Connect the circuit shown in Figure.
2. Ensure that the variable DC is at minimum and the source is at 10VP.P.
3. Observe and Sketch the input and output waveforms.
4. Increase the variable DC voltage to 4V, and notice to what voltage are the Positive peaks chopped off, sketch the waveforms.

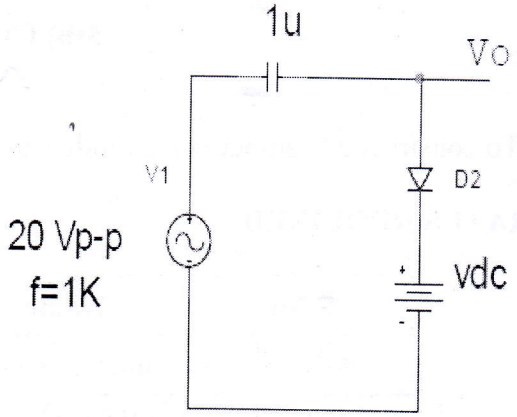
Result:

Thus the static characteristics clipper configuration is studied.

Result:

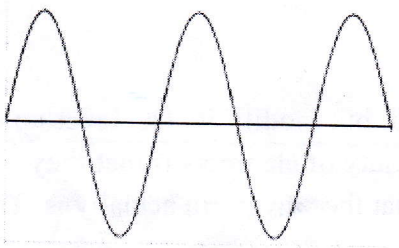
Thus the static characteristics clamper configuration is studied.



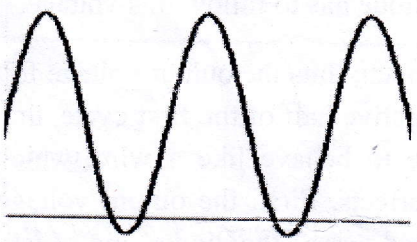


Model Graph:

Input Characteristics:



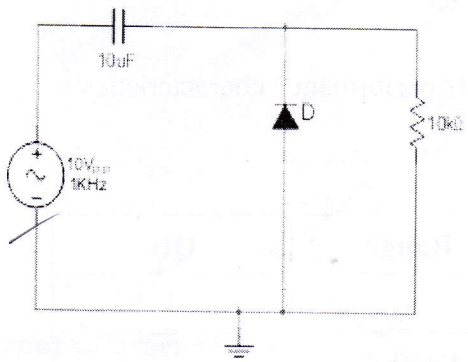
Output characteristics:

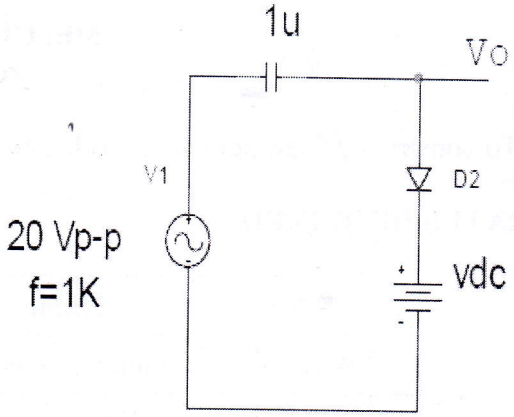


C

Procedure:

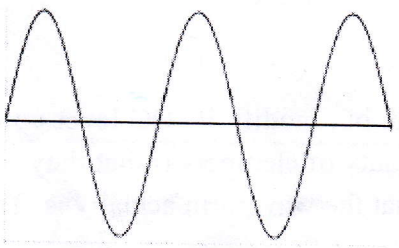
1. Connect the circuit shown in Figure.
2. Ensure the variable DC is at minimum.
3. Set the sine wave generator frequency to 1KHz and its output amplitude to 10VP.P
4. Observe and sketch the input waveform with the variable DC at minimum,
5. Sketch the output waveform.



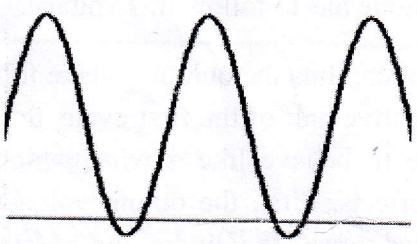


Model Graph:

Input Characteristics:



Output characteristics:



C

Procedure:

1. Connect the circuit shown in Figure.
2. Ensure the variable DC is at minimum.
3. Set the sine wave generator frequency to 1KHz and its output amplitude to 10VP.P
4. Observe and sketch the input waveform with the variable DC at minimum,
5. Sketch the output waveform.

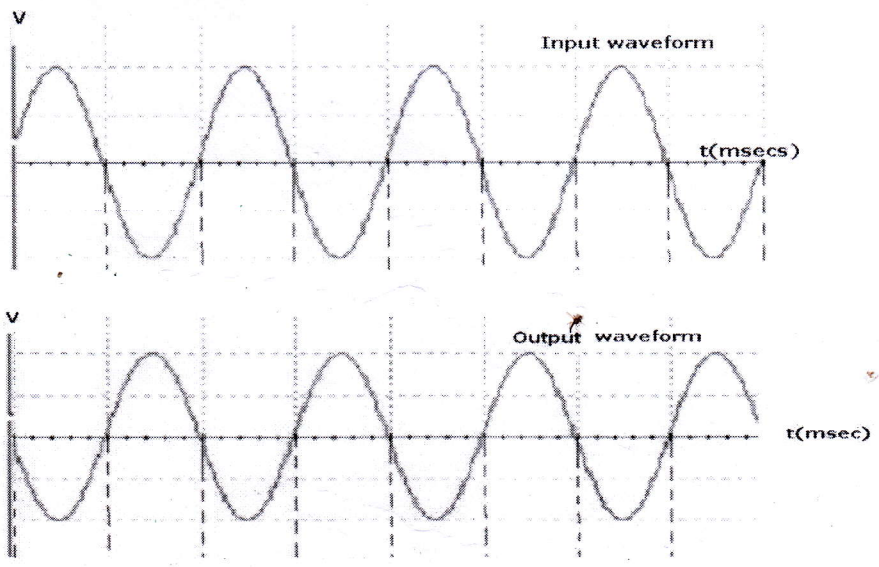
1. Connections are made as per circuit diagram.
2. Keep the input voltage constant at 20mV peak-peak and 1kHz frequency.For different values of load resistance, note down the output voltage
3. Calculate the gain by using the expression$A_v = 20\log(V_0 / V_i)$ dB
4. Remove the emitter bypass capacitor and repeat STEP 2.And observe the effect of feedback on the gain of the amplifier.
5. For plotting the frequency the input voltage is kept constant at 20mV peak-peak and the frequency is varied from 100Hz to 1MHz.
6. Note down the value of output voltage for each frequency.
7. All the readings are tabulatedand the voltage gain in dB is calculated by using expression
   $A_v = 20\log (V_0 / V_i)$ dB
8. A graph is drawn by taking frequency on X-axis and gain on Y-axis on semi log graph

9. The Bandwidth of the amplifier is calculated from the graph using the expression Bandwidth B.W = $f_2 - f_1$.
   a. Where f_1 is lower cutt off frequency of CE amplifier f_2 is upper cutt off frequency of CE amplifier

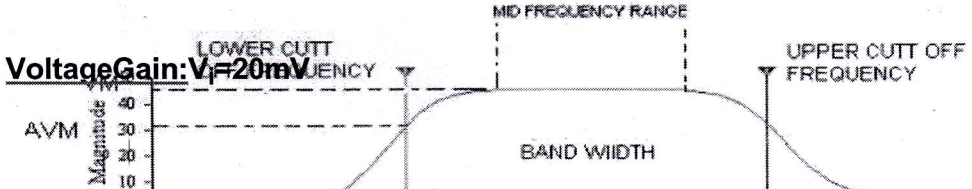
10. The gain-bandwidth product of the amplifier is calculated by using the expression

    i. Gain-Bandwidth Product = 3-dB midband gain X Bandwidth.

ModelGraph:



TabularColums:



7.VOLTAGESERIESFEEDBACKAMPLIFIER

Aim:

To plot the frequency response characteristics of voltage series feedback amplifier.

ApparatusRequired:

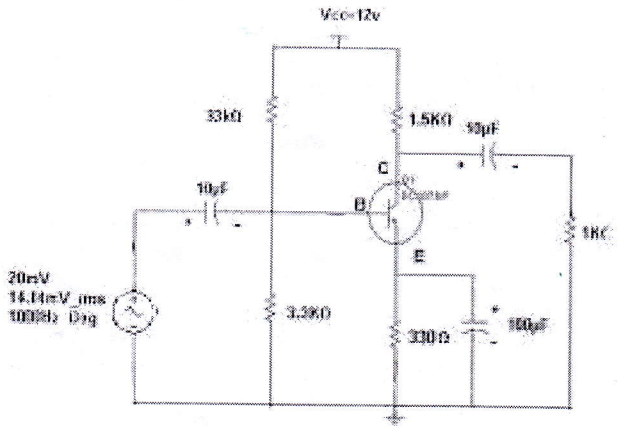
Transistor

Resistorsandcapacitors,

Functiongenerator,

CRO

CircuitDiagram:



THEORY:

When anyincreaseintheoutputsignalresultsintotheinputinsuchawayastocausethedecreaseintheoutputsignal,theamplifierissaidtohavenegativefeedback.

The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistoror the parameters of the other active devices used in the circuit.Th emost advantage of the negative feedback is thatby proper use of this,there issignificant improvement int he frequency response andi n the linearityof the operation of the amplifier.This disadvantage oft he negative feedback is that the voltage gain is decreased.InCurrent-SeriesFeedback,theinput impedance and the output impedance are increased.Noise and distortions are reduced considerably.

PROCEDURE:

S.NO	Output Voltage (V_o) with feedback	Output Voltage (V_o) without feedback	Gain(dB)with feedback	Gain(dB) without feedback

PRECAUTIONS:

Whiletakingtheobservationsforthefrequencyresponse,theinputvoltagemustbemaintainedconstantat20mV.

Thefrequencyshouldbeslowlyincreasedinsteps.

Thethreeterminalsofthetransistorshouldbecarefullyidentified.

Alltheconnectionsshouldbecorrect.

RESULT:

Thus voltage series feedback amplifieris realised.

EXPERIMENT 7: STUDY OF RC PHASE SHIFT OSCILLATOR.

AIM:

To design and set up an RC phase shift oscillator using BJT and to observe the sinusoidal output waveform.

APPARATUS REQUIRED:

S.NO.	NAME OF THE EQUIPMENT	TYPE	RANGE	QUANTITY (NO.S)
1	*Transistor*	BC547		1
2	*Resistors*		47kΩ, 10kΩ,2.2kΩ,680Ω	*one from each*
3	*Resistor*		4.7kΩ	*3*
3	*Capacitors*		1µF,22µF	*one from each*
4	*Capacitor*		0.01 µF	3
5	*CRO*			
6	*RPS*		(0 – 30V)	1
7	*Bread Board*			1
8	*Connecting wires*			Required

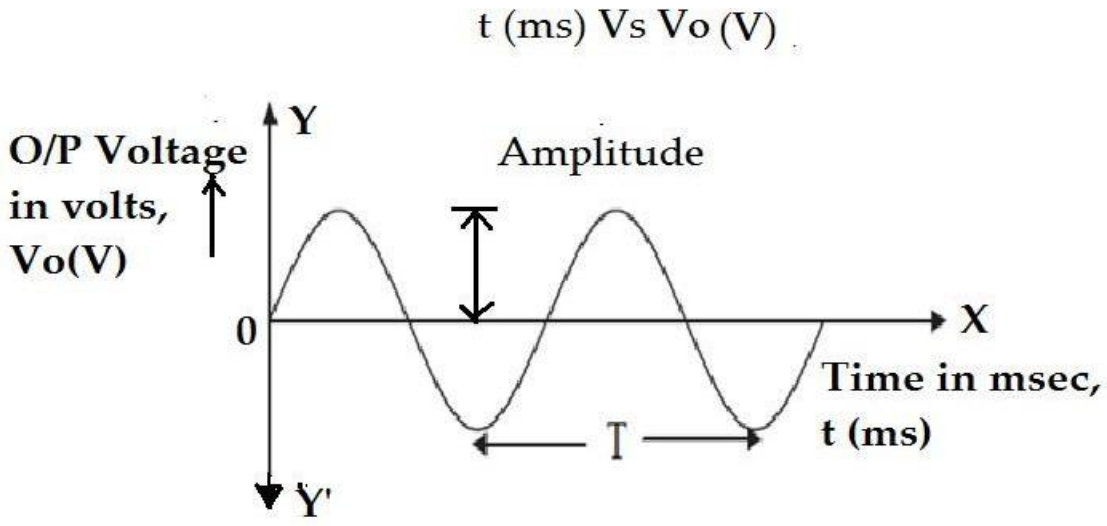
THEORY:

An oscillator is an electronic circuit for generating an AC signal voltage with a DC supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements used. An oscillator requires an amplifier, a frequency selective network and a positive feedback from the output to the input.

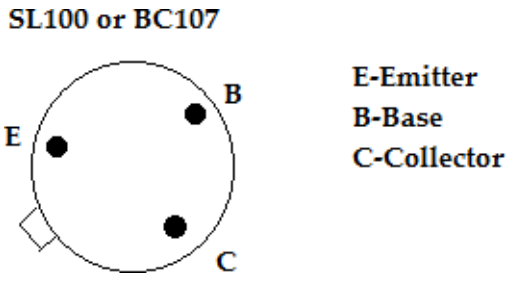
The Barkhausen criterion for sustained oscillation is $A\beta = 1$ where A is the gain of the amplifier and β is the feedback factor (gain).The unity gain means signal is in phase. (If the signal is 180^{o} out of phase and gain will be -1). RC-Phase shift Oscillator has a CE amplifier followed by three sections of RC phase shift feed-back Networks. The output of the last stage is return to the input of the amplifier. The values of R and C are chosen such that the phase shift of each RC section is 60º.Thus The RC ladder network produces a total phase shift of 180º between its input and output voltage for the given frequency. Since CE Amplifier produces 180 º phases shift. The total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360º or 0º. This satisfies the Barkhausen condition for sustaining oscillations and total loop gain of this circuit is greater than

or equal to 1, this condition used to generate the sinusoidal oscillations.

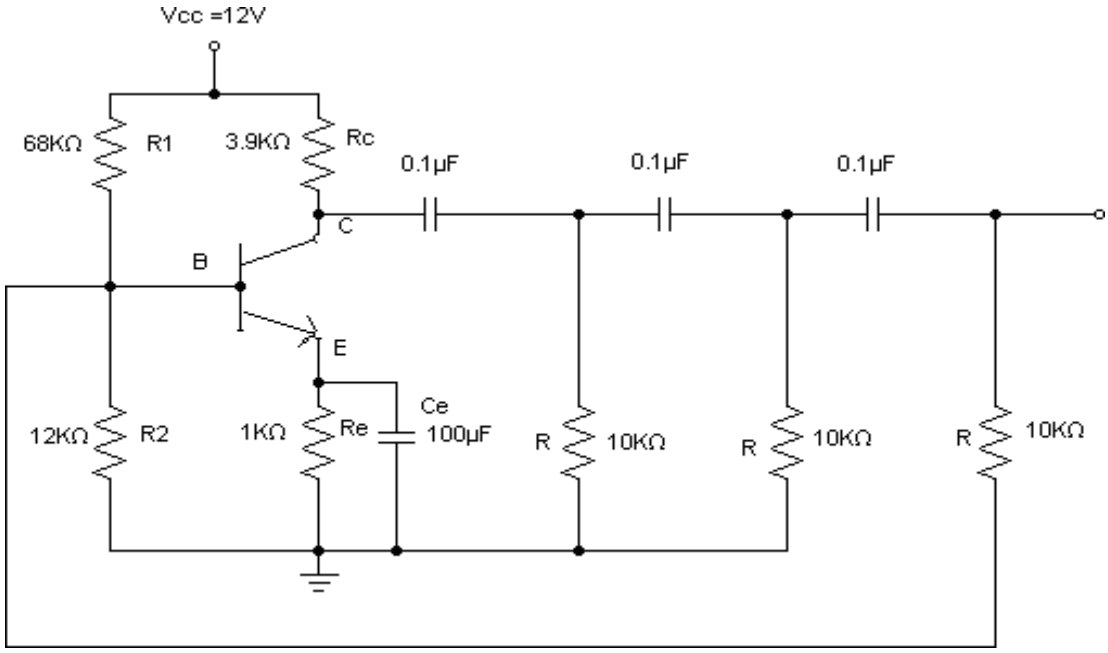
MODEL GRAPH:



BJT PIN DIAGRAM



CIRCUIT DIAGRAM:



PROCEDURE:

1. Identify the pin details of BC107 Transistor (or equivalent silicon Transistor such as BC108/547) and test it using a millimeter. Set up the circuit on breadboard as shown in figure.
2. A 12V Supply Voltage is given by using Regulated power supply and output is taken from collector of the Transistor.
3. By using CRO the output time period and voltage are noted.
4. Plot all the readings curves on a single graph sheet.

RESULT:

Thus the RC phase shift oscillator using BJT was obtained and the output waveform was plotted.

Experiment No:8a

COMMON COLLECTOR AMPLIFIER

AIM: - To Study the common collector amplifier and to find

1. Cut off frequencies.
2. Bandwidth.

Components:

Name	Qty
Transistor BC 107	1
Resistors 10KΩ,33KΩ,8.2KΩ,2.2KΩ	1
Capacitors 10µf	2

EQUIPMENT REQUIRED:

Equipment	Quantity
Bread Board	1
CRO	1
Function generator	1
Connecting Wires	

THEORY:

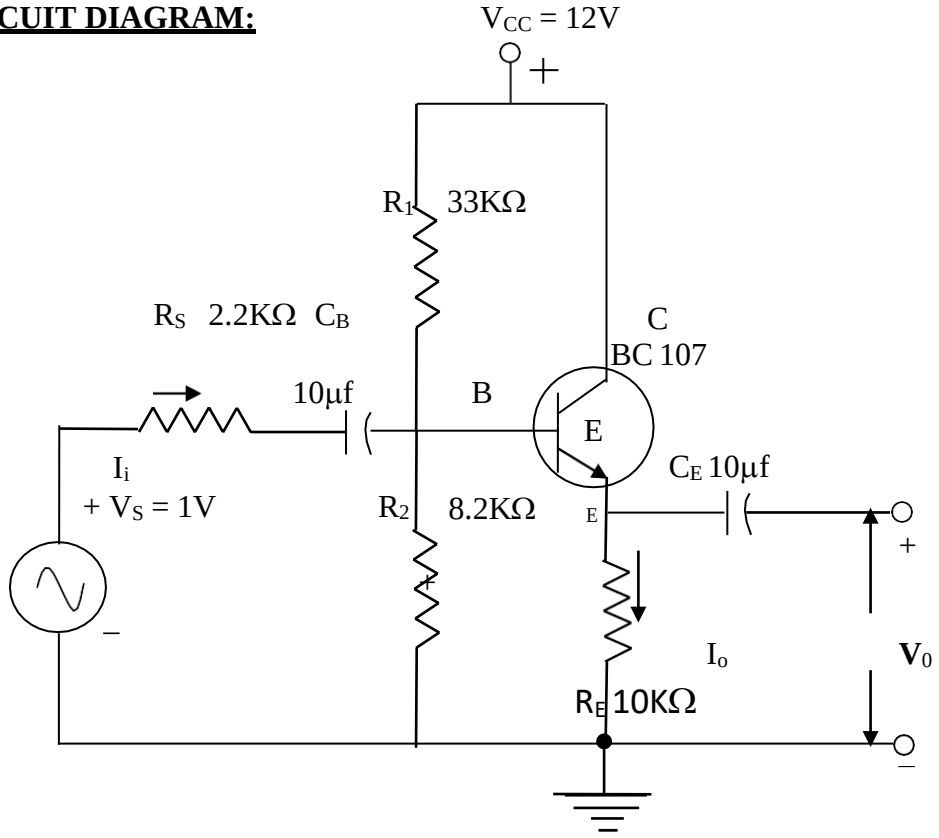
In common collector amplifier as the collector resistance is made to zero, the Collector is at ac ground that is why the circuit is also called as grounded Collector amplifier or this configuration is having voltage gain close to unity And hence a change in base voltage appears as an equal change across the Load at the emitter, hence the name emitter follower. In other words the Emitter follows the input signal.

This circuit performs the function of impedance transformation over a wide range of frequencies with voltage gain close to unity. In addition to that, the emitter follower increases the output level of the signal. Since the output voltage across the emitter load can never exceed the input voltage to base, as the emitter-base junction would become back biased. Common collector state has a low output resistance, the circuit suitable to serve as buffer or isolating amplifier or couple to a load with large current demands.

Characteristics of CC amplifier:

1. Higher current gain
2. Voltage gain of approximately unity
3. Power gain approximately equal to current gain
4. No current or voltage phase shift
5. Large input resistance
6. Small output resistance

CIRCUIT DIAGRAM:

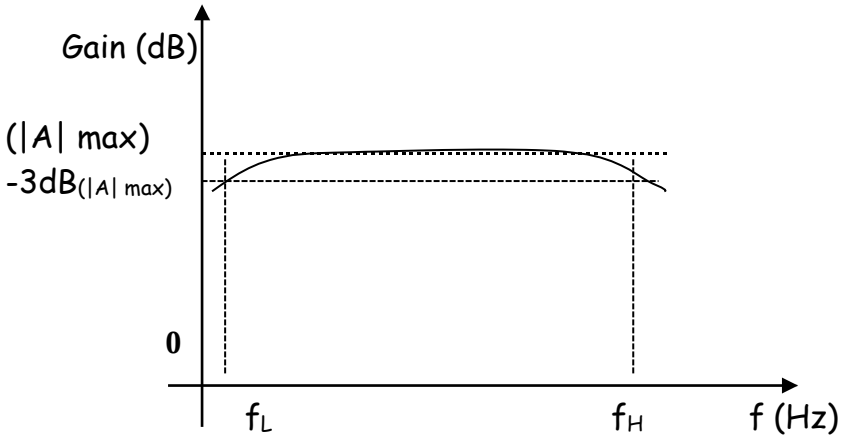


PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage V_s = 50mV (say) at 1 KHz frequency, using function generator.
3. keeping the input voltage constant vary the frequency from 50Hz to 1MHz in regular steps

   And note down the corresponding output voltage.
4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.

Graph (Frequency Response):



TABULAR COLUMN: **V_S = 50mV**

In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L and f_H, and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth ($f_H - f_L$).

RESULT:

Maximum Gain=

3db Gain= Maximum Gain -3db

Band Width =

Viva Voce Questions

1. Why CC amplifier is known as emitter follower?
2. Mention the applications of CC amplifier. Justify?
3. What is the phase difference between input and output signals in the case of CC amplifier?
4. Mention the characteristics of CC amplifier?
5. What is gain bandwidth product?

Frequency	**V_O (volts)**	**Gain = V_o/V_s**	**Gain (dB) =20 $\log_{10}$ V_o/V_s)**

Experiment No: 8b
COMMON EMITTER AMPLIFIER

AIM: - To Study the common emitter amplifier and to find
1. Cut off frequencies.
2. Bandwidth.

Components:

Name	Qty
Transistor BC 107	1
Resistors 10KΩ(2),33KΩ,1KΩ	1
Capacitors 10µf	2
4.7 µf (1)	

EQUIPMENT REQUIRED:

Name	Qty
Bread Board	1
CRO	1
Function generator	1
Connecting wires	

THEORY:
The common emitter configuration is widely used as a basic amplifier as
It has both voltage and current amplification.

Resistors R_1 & R_2 form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and, ensure that emitter - base junction is operating in the proper region.

In order to operate transistor as an amplifier, the biasing is done in such a way that the operating point should be in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design the V_{CE} is always set to $V_{CC}/2$. This will conform that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. Output is produced without any clipping or distortion for the maximum input signal. If not so, reduce the input signal magnitude.

The Bypass Capacitor The emitter resistor R_E is required to obtain the DC quiescent stability. However the inclusion of R_E in the circuit causes a decrease in amplification at higher frequencies. In order to avoid such a condition, it is bypassed by capacitor so that it acts as a short circuit for AC and contributes stability for DC quiescent condition. Hence capacitor is connected in parallel with emitter resistance.

$$X_{CE} << R_E$$

$$\frac{1}{2\pi f C_E} << R_E$$

$$C_E >> \frac{1}{2\pi f R_E}$$

The Coupling Capacitor An amplifier amplifies the given AC signal. In order to have noiseless transmission of signal (with out DC), it is necessary to block DC i.e. the direct current should not enter the amplifier or load. This is usually accomplished by inserting a coupling capacitor between any two stages.

$$X_{CC} << (R_i \quad hie)$$

$$\frac{1}{2\pi f C_C} << (Ri \quad hie)$$

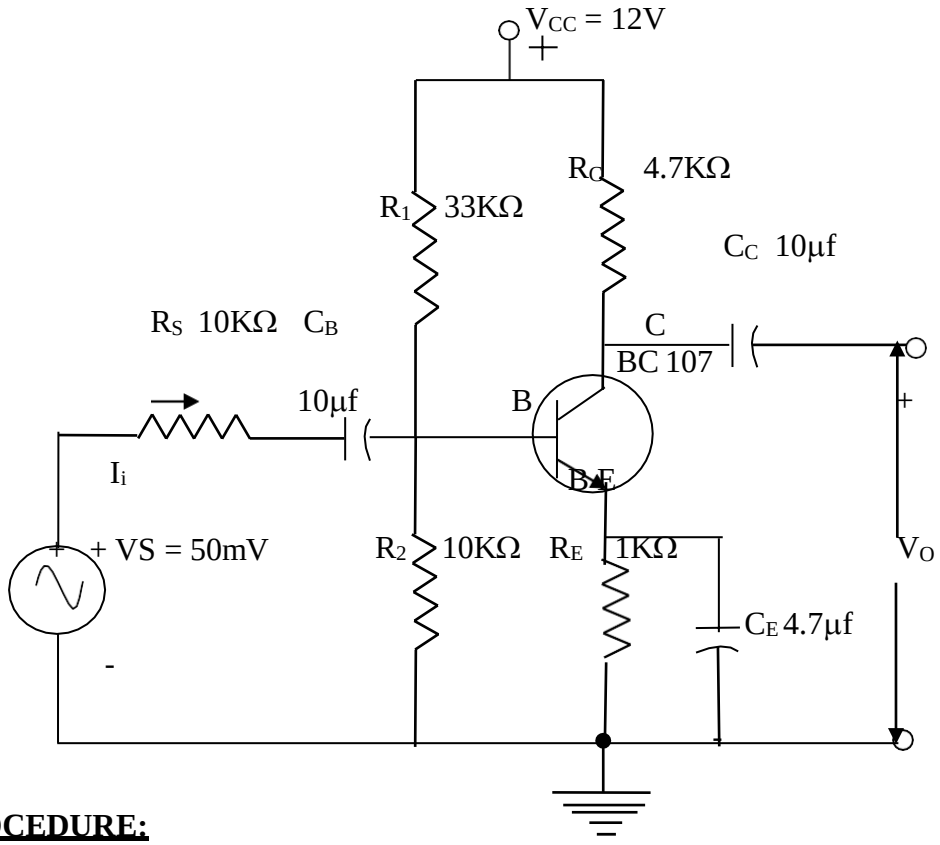
$$C_C >> \frac{1}{2\pi f C_C (Ri \quad hie)}$$

Frequency Response Emitter bypass capacitors are used to short circuit the emitter resistor and thus increase the gain at high frequency. The coupling and bypass capacitors cause the fall of in the low frequency response of the amplifier because their impedance becomes large at low frequencies. The stray capacitors are effectively open circuits.

In the mid frequency range the large capacitors are effective short circuits and the stray capacitors are open circuits, so that no capacitance appears in the mid frequency range. Hence, the mid band gain is maximum.

At the high frequencies, the bypass and coupling capacitors are replaced by short circuits and stray capacitors and the transistor determine the response.

CIRCUIT DIAGRAM:



PROCEDURE:

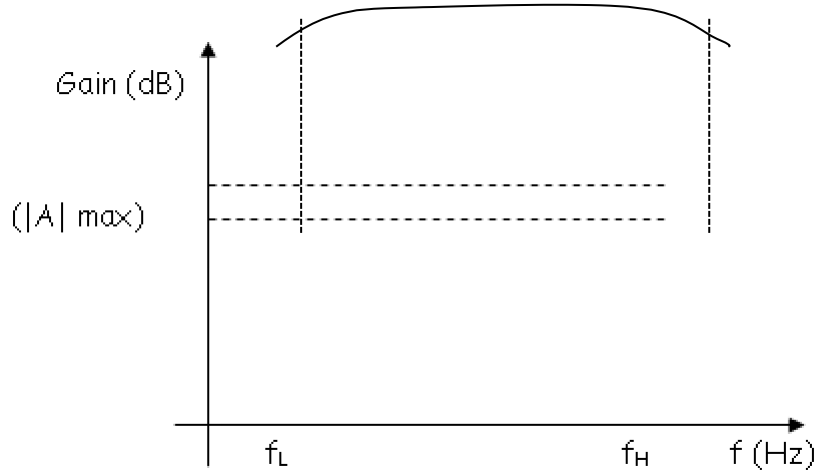
1. Connect the circuit as per the circuit diagram.
2. Set Source Voltage V_s = 50mV (say) at 1 KHz frequency, using function generator.
3. Keeping the input voltage constant vary the frequency from 50Hz to 1MHz in regular steps and note down the corresponding output voltage.

4. Plot the Graph: gain (dB) Vs frequency.
5. Calculate the bandwidth from Graph.
6. Calculate all the parameters at mid band frequencies (i.e. at 1 KHz).

Graph (Frequency Response):
TABULAR COLUMN:

Frequency	**V_O (volts)**	**Gain = V_o/V_s**	**Gain (dB) =20 log (V_o/V_s)**

V_S = 50mV



In the usual application, mid band frequency range are defined as those frequencies at which the response has fallen to 3dB below the maximum gain (|A| max). These are shown as f_L and f_H, and are called as the 3dB frequencies are simply the lower and higher cut off frequencies respectively. The difference between higher cut-off frequency and lower cut-off frequency is referred to as bandwidth ($f_H - f_L$).

RESULT

Maximum Gain=
3db Gain= Maximum Gain -3db

Band Width =

Reasoning Questions

1. How do we test the transistor for active region condition?
2. What are the factors, which influence the higher cut-off frequency?
3. What are the components, which influence the lower cut-off frequency?

4. Mention the applications of CE amplifier. Justify?
5. Compare the characteristics of CE amplifier, CB amplifier & CC amplifier.
6. What must be the voltage across the transistor, when it is operated as a switch?
7. How do we test the transistor for switching condition?

9 TUNED VOLTAGE AMPLIFIER

Exp. No: Date:

PREAMBLE:

Study the operation and working principle Tuned amplifier.

OBJECTIVE:

To obtain the frequency response of a tuned voltage amplifier using Multisim and to obtain the band width.

SOFTWARE TOOL:

- Multisim

APPARATUS:

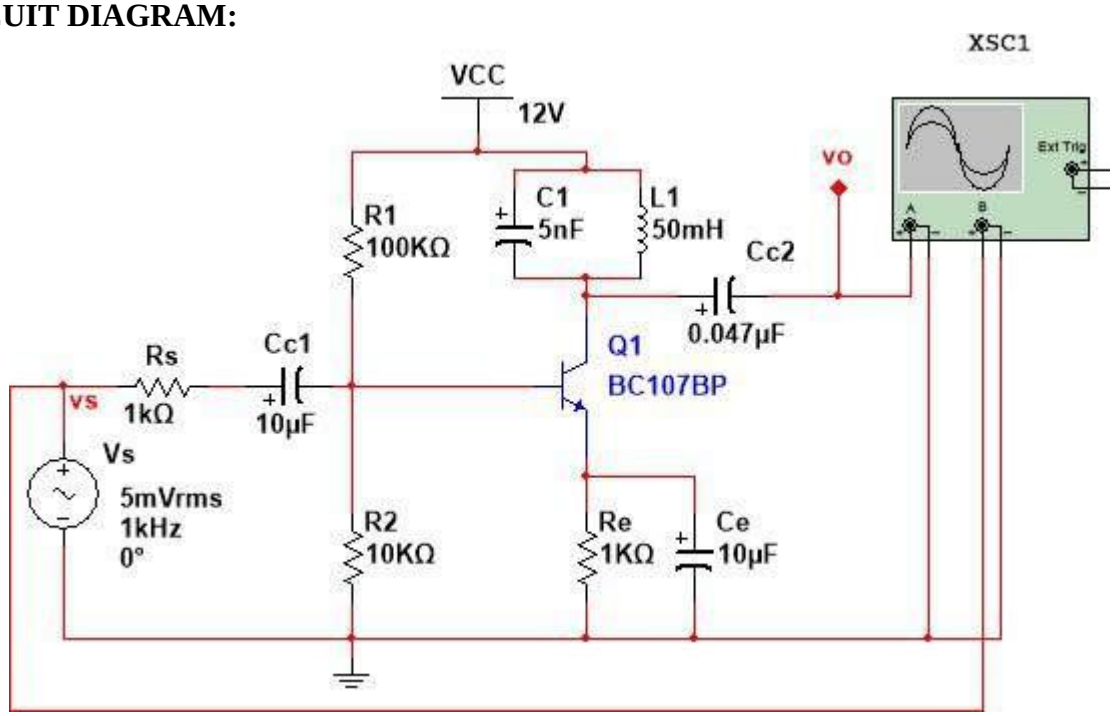
S. No	Name	Range / Value	Quantity
1	Transistor	SL100/BC 107	1
2	Resistors	1KΩ ,100KΩ,10kΩ	2,1,1
3	Capacitors	10uF,5nf,0.047uf	2,1,1
4	Inductor	50mH	1
5	RPS	12V	1
6	CRO	30MHz	1

THEORY:

Most of the audio amplifiers we have discussed in the earlier chapters will also work at radio frequencies i.e. above 50 kHz. However, they suffer from two major drawbacks. First, they become less efficient at radio frequency. Secondly, such amplifiers have mostly resistive loads and consequently their gain is independent of signal frequency over a large bandwidth. In other words, an audio amplifier amplifies a wide band of frequencies equally well and does not permit the selection of a particular desired frequency while rejecting all other frequencies. However, sometimes it is desired that an amplifier should be selective i.e. it should select a desired frequency or narrow band of frequencies for amplification.

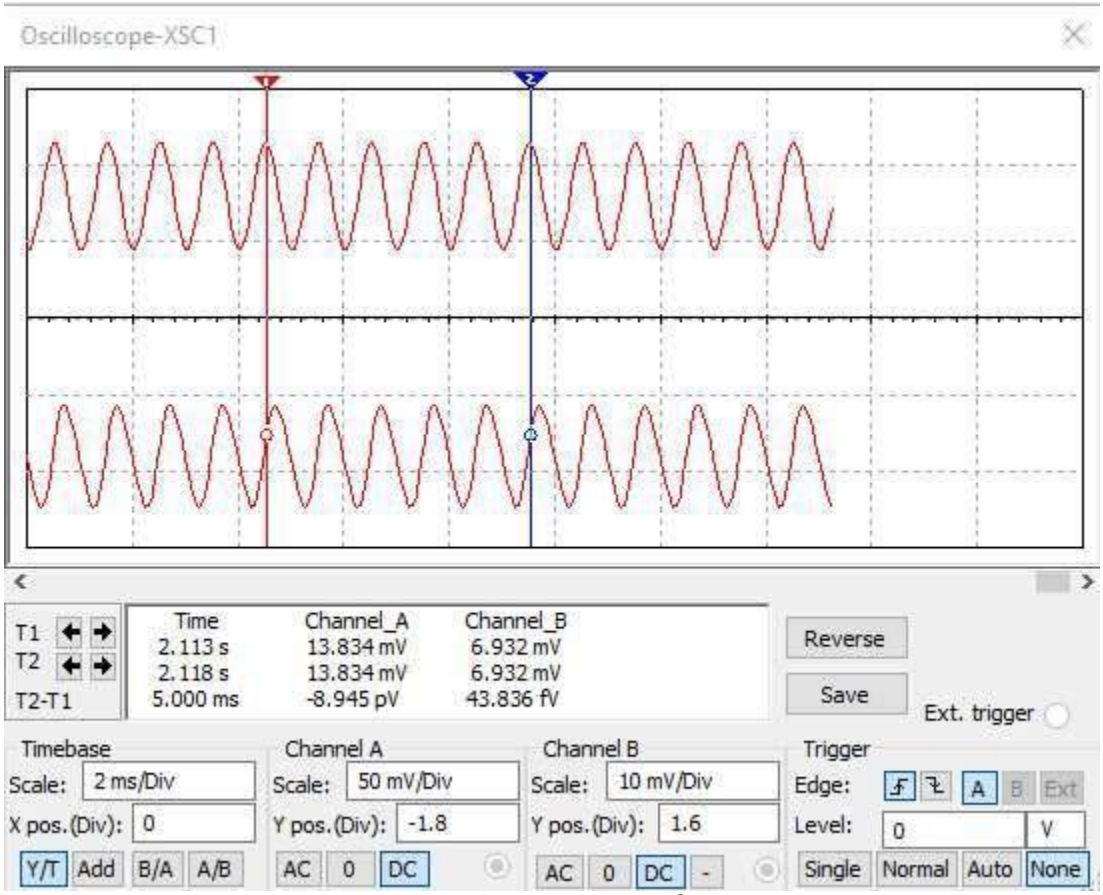
For instance, radio and television transmission are carried on a specific radio frequency assigned to the broadcasting station. The radio receiver is required to pick up and amplify the radio frequency desired while discriminating all others. To achieve this, the simple resistive load is replaced by a parallel tuned circuit whose impedance strongly depends upon frequency. Such a tuned circuit becomes very selective and amplifies very strongly signals of resonant frequency and narrow band on either side. Therefore, the use of tuned circuits in conjunction with a transistor makes possible the selection and efficient amplification of a particular desired radio frequency. Such an amplifier is called a tuned amplifier. In this chapter, we shall focus our attention on transistor tuned amplifiers and their increasing applications in high frequency electronic circuits.

CIRCUIT DIAGRAM:



TUNED VOLTAGE AMPLIFIER

OBSERVATIONS/GRAPHS:



Input and Output waveforms

Amplifiers which amplify a specific frequency or narrow band of frequencies are called tuned amplifiers. Tuned amplifiers are mostly used for the amplification of high or radio frequencies. It is because radio frequencies are generally single and the tuned circuit permits their selection and efficient amplification. However, such amplifiers are not suitable for the amplification of audio frequencies as they are mixture of frequencies from 20 Hz to 20 kHz and not single. Tuned amplifiers are widely used in radio and television circuits where they are called upon to handle radio frequencies. Below figure shows the circuit of a simple transistor tuned amplifier. Here, instead of load resistor, we have a parallel tuned circuit in the collector. The impedance of this tuned circuit strongly depends upon frequency. It offers a very high impedance at resonant frequency and very small impedance at all other frequencies. If the signal has the same frequency as the resonant frequency of LC circuit, large amplification will result due to high impedance of LC circuit at this frequency. When signals of many frequencies are present at the input of tuned amplifier, it will select and strongly amplify the signals of resonant frequency while rejecting all others. Therefore, such amplifiers are very useful in radio receivers to select the signal from one particular broadcasting station when signals of many other frequencies are present at the receiving aerial.

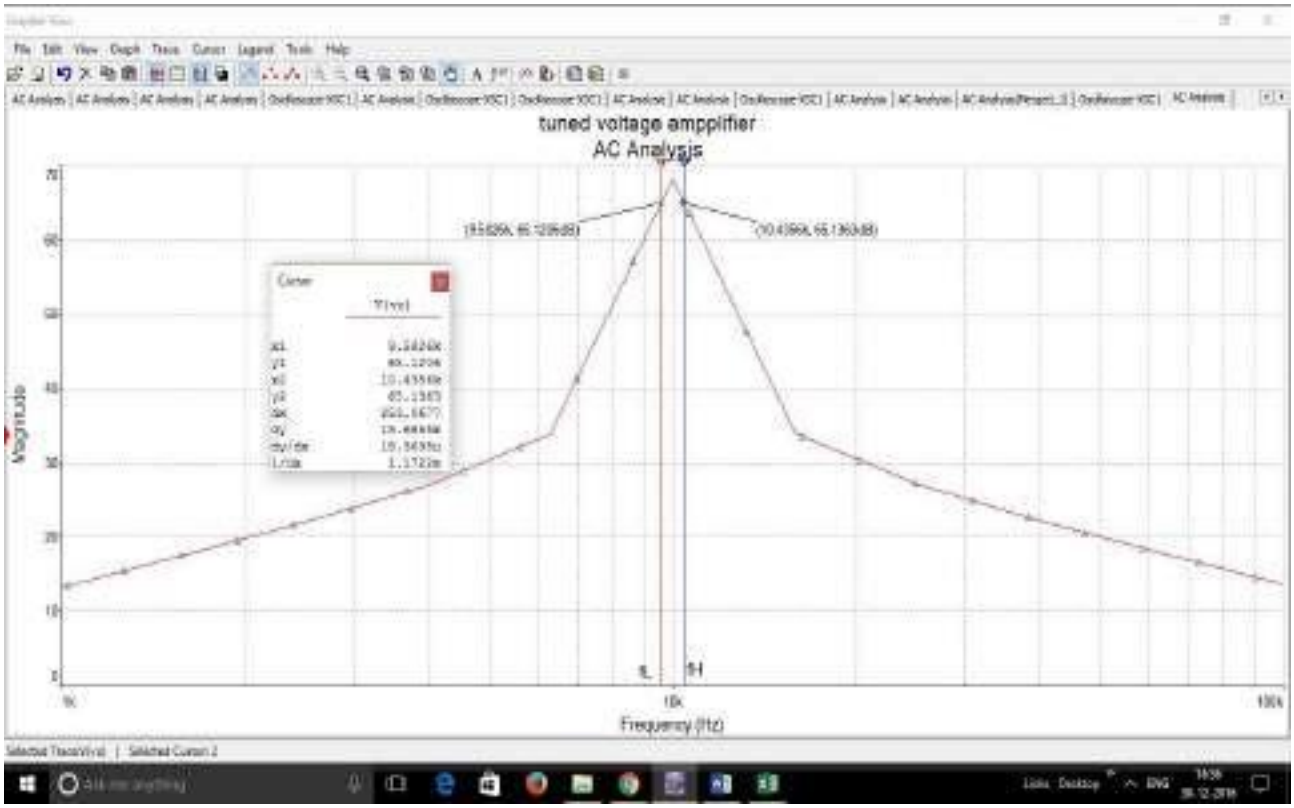
PROCEDURE:

1. Open Multisim Software to design circuit
2. Select on New editor window and place the required component on the circuit window.
3. Make the connections using wire and check the connections and oscillator.
4. Go for simulation and using Run Key observe the output waveforms on CRO
5. Indicate the node names and go for AC Analysis with the output node
6. Observe the Ac Analysis and draw the magnitude response curve
7. Calculate the bandwidth of the amplifier

RESULT &DISCUSSION:

1. Frequency response of single tuned Amplifier is pSetted.
2. Gain =_____dB (maximum).
3. Bandwidth= (fH—fL) =_____Hz.

Frequency Response:



Theoretical calculations:

REVIEW QUESTIONS:

1. What is a tuned amplifier?
2. Define Q-factor?
3. What is selectivity?
4. Is tuned amplifier a hallow band or wide band amplifier?
5. Give the applications for tuned amplifier.

***

HOD/ EEE
Dr. L. Chitra