1.Measurements of Op-Amp parameters

AIM: To measure the following parameters of an op- amp

1. CMRR
2. slew rate
3. Input bias current
4. Input offset current .

Components and Equipments required: Power supplies, CRO, function generator, op- amp, resistor ,capacitors & bread board.

THEORY:

1.*CMRR*- It is the ratio of differential mode gain to common mode gain . If a signal is applied common to both the inputs of op –amp , signal will be attenuated. CMRR is usually expressed in *dB*. When an input signal Vs is applied, common to both inputs , common mode voltage gain $Ac = Vo/Vs$. Differential mode gain

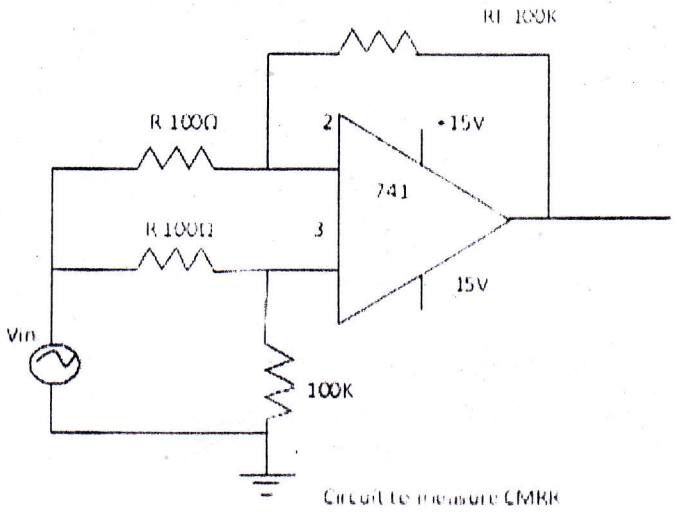
$Ad = Rf/Ri$. Then *CMRR* is given by the expression CMRR $= 20 \log (Ad/Ac)$ in *dB*

2.Slew rate – slew rate is the maximum rate of rise of output voltage. It is the measure of fastness of op- amp. It is expressed in *V/μs*. The internal output capacitance prevents sudden rise of output voltage for a fast rising input . If the slope requirements of the output voltage of the op-amp is greater than the slew rate, distortion occurs.

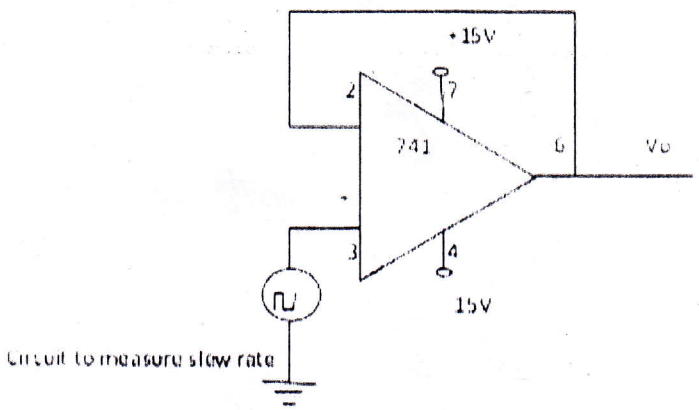
3.Input bias current I_B :

The inverting and non inverting non inverting terminals of an opamp are two base terminals of the transistors of a differential amplifier. In an ideal op-amp no

CIRCUIT DIAGRAMS



Circuit to measure CMRR



Circuit to measure slew rate

current flows through these terminals . However , a small amount of current flows through these terminals which is of the order of *n*A in bipolar op- amps and pA for FET pA for FET op-Amp's .

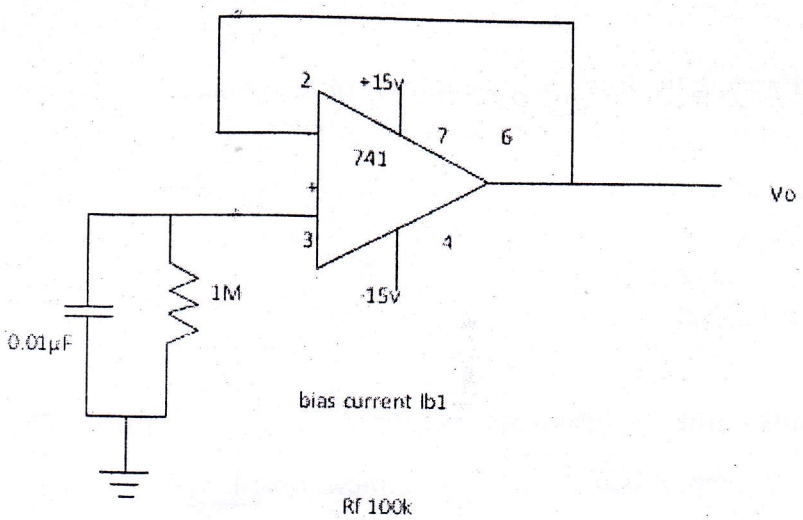
Input bias current is defined as the average of the currents entering in to the inverting and noninverting terminals of an opamp. To compensate for bias currents, a compensating resistor Rcomp is used. Value of Rcomp is the parallel combination of the resistors connected to the inverting terminal.

Input Bias current $I_B = (I_{B1} + I_{B2})/2$ where I_{B1} and I_{B2} are the base bias currents of the op-amp.

5. Input offset current I_{OS}:

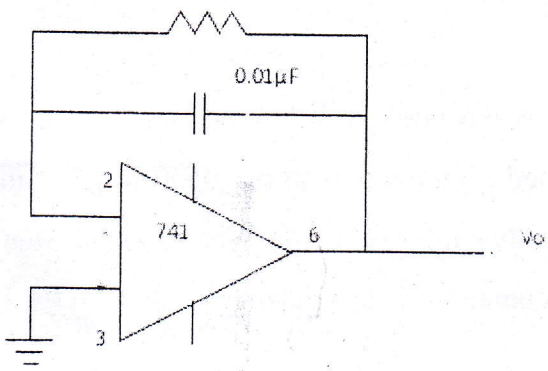
   The bias currents I_{B1} and I_{B2} are not equal in an opamp. Input offset current is defined as the algebraic difference between the currents into the inverting and noninverting terminals . Typical and maximum values of offset current are 20*nA* and 200 *nA*

$$\text{Input offset current } I_{OS} = \left| I_{B1} - I_{B2} \right|$$



bias current Ib1

Rf 100k



bias current Ib2

PROCEDURE:

1) Setup the circuit for finding CMRR. Apply a dc signal of 0.5 V at the input and measure Vo. Calculate CMRR using the expression

$$CMRR = \frac{Vi(Rf/Ri)}{Vo}$$

Express CMRR in dB using the expression 20log(CMRR)

2) Feed a square wave to input and calculate slew rate using the expression

SR = ΔVo/t; where ΔVo is the voltage swing and t is the time taken to change the voltage levels

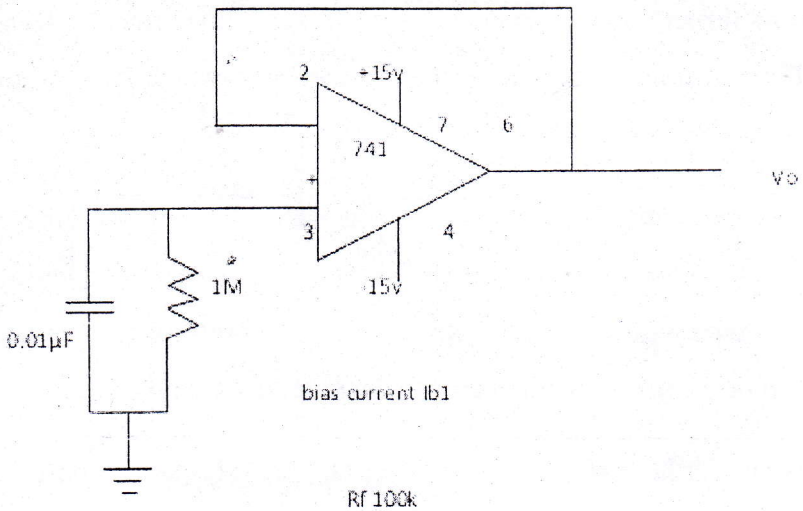
3)Set up the circuits for measuring input bias current and input offset current. Measure the output voltage . Using the expression $Vo = I_{B1}R$ and $Vo = I_{B2}R$. IB1 and IB2 are calculated. Use the expression

$$I_B = (I_{B1} + I_{B2})/2 ,$$

$$I_{OS} = I_{B1} - I_{B2}$$

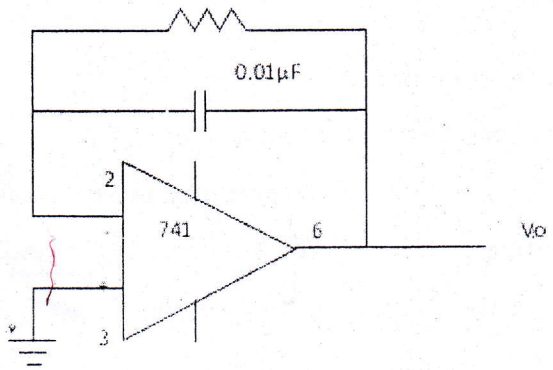
RESULT:

Measured the parameters of an Op- Amp.



bias current Ib1

Rf 100k



bias current Ib2

2. INVERTING, NONINVERTING, INTEGRATOR AND DIFFERENTIAOR AMPLIFIER

AIM:

To study the operation of inverting non-inverting, integrator and Differentiator amplifier using IC741.

APPRATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QUANTITY
1	Op-amp	IC741	1
2	Resistor	1kΩ,10 kΩ	1
3	Bread board		1
4	Dual power supply	(0-30)v	1
5	CRO	(0-3) MHz)	1
6	Signal generator	(0-3) MHZ	1

INVERTING AMPLIFIER:

THEORY:

An amplifier which provides a phase shift of 180° between input and output is called inverting amplifier. The input signal is applied to the inverting terminal In this mode of operation the positive input terminal of an amplifier is grounded and the input voltage is applied to the negative input terminal through resistor R_1 .The feedback applied through resistor R_f from the output to the negative input terminal. The output of such amplifier is inverted as compared to the input terminal.

$A = -R_f/R_1$

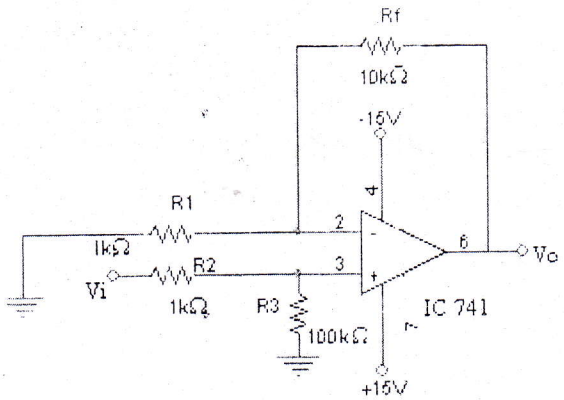
R_f=Feedback resistor

R_1= input resistor

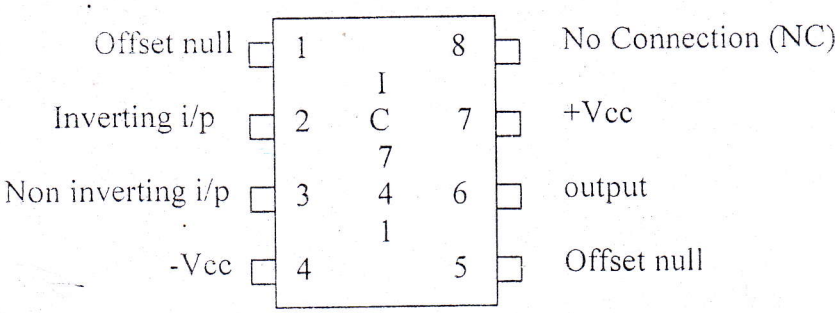
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Connect the dual supply voltage of -15v and +15v to op-amp
3. Set the i/p voltage.
4. Using the probes obtain the input from the CRO. Tabulate the voltage and time period

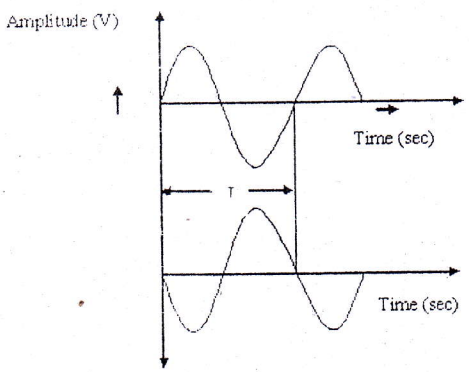
CIRCUIT DIAGRAM:



PINDETAILS



MODEL GRAPH



TABULATION

	Amplitude (volts)	Time period (ms)
Input		
Output		

5. using the probes obtain the output from the CRO .Tabulate the voltage and time Period, compare with the input.

6. Plot the graph between the voltage on the x axis and time period on the y axis.

NON - INVERTING AMPLIFIER

THEORY:

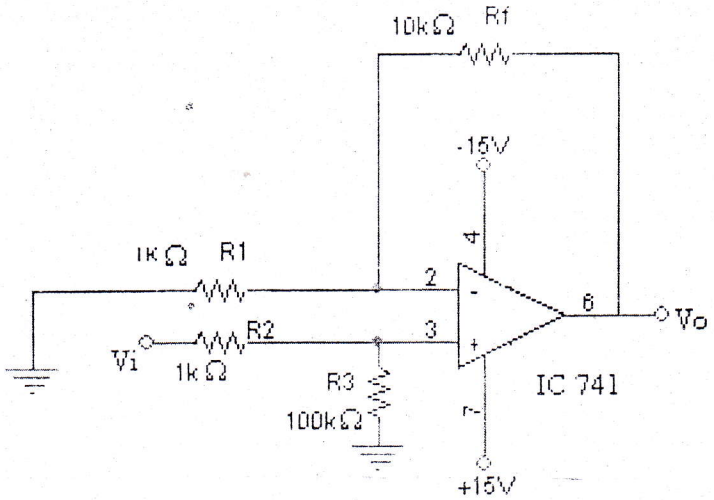
An amplifier which amplifies the input without producing any phase shift between input and output is called non – inverting amplifier. The input is applied to the non inverting terminal of the op-amp. In this mode of operation the Negative input terminal of an amplifier is grounded and the input voltage is applied to the Positive input terminal through resistor R_1 .

$$V_O = (1 + R_f/R_1)V_{In}$$

PROCEDURE:

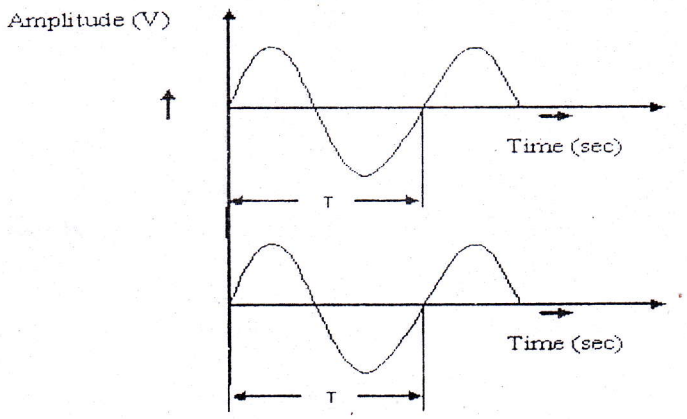
1. Connections are given as per the circuit diagram.
2. Connect the dual supply voltage of -15v and +15v to op-amp
3. Set the i/p voltage.
4. using the probes obtain the input from the CRO.
5. using the probes obtain the output from the CRO .Tabulate the voltage and time period. compare with the input.
5. Plot the graph. Plot the graph between the voltage on the x axis and time period on the y axis.

CIRCUIT DIAGRAM:



Non - inverting amplifier

MODEL GRAPH



I/P&0/P Waveforms

TABULATION

	Amplitude (volts)	Time (ms)
Input		
Output		

INTEGRATOR

THEORY

In an integrator circuit, the output voltage is the integration of the input voltage. The integrator using an active device like op – amp is called as an active integrator. The limitations of an ideal integrator can be minimized by the practical integrator circuit which uses resistance in parallel with the capacitor.

A I circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or the integration amplifier.

$$Vo=1/R1C1 * \int_0^t vin\ dt + c$$

V_o = output voltage

R_1 = input resistance

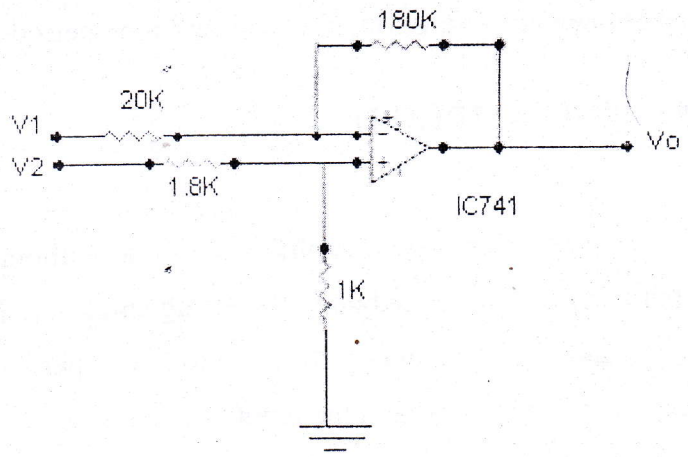
C_F = feedback capacitor

v_{in} = input voltage

PROCEDURE:

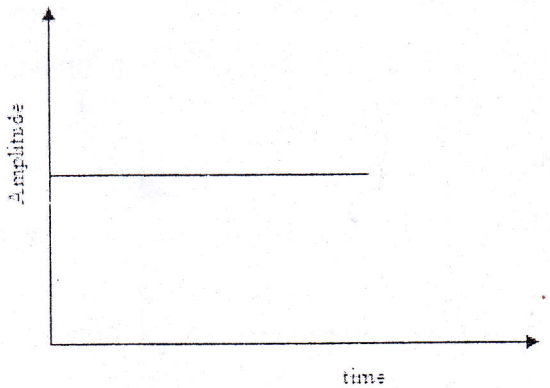
1. Connections are made as per the circuit diagram.
2. Connect the dual supply voltage of +15V and -15V to bias the Opamp.
3. A Sine wave of 1Vpp at 2KHz is given as input to pin 2.
4. A Sine wave of 1.5Vpp at 2KHz is given as input to pin 3.
4. using the probe obtain the Output waveform from the CRO.
5. Amplitude and time period readings are tabulated.
6. Plot the graph between the voltage on the x axis and time period on the y axis.

CIRCUIT DIAGRAM



Differential Amplifier

MODEL GRAPH



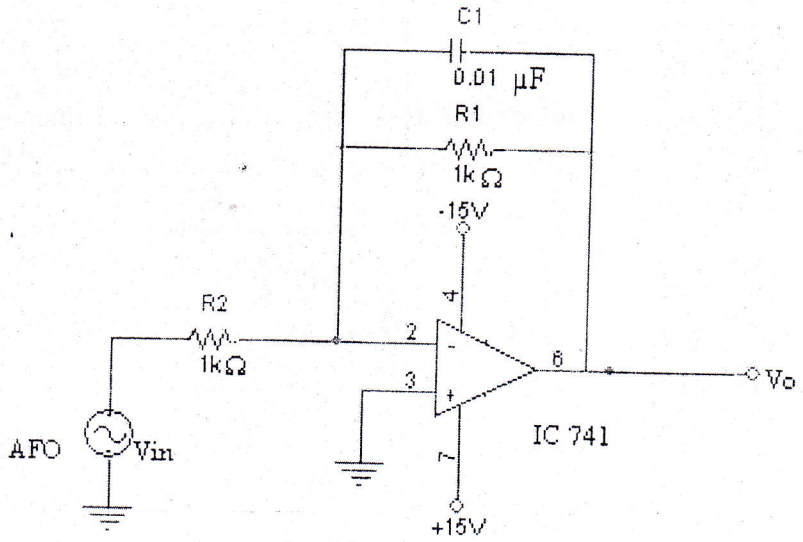
TABULATION

	Amplitude (volts)	Time (ms)
Input		
Output		

RESULT:

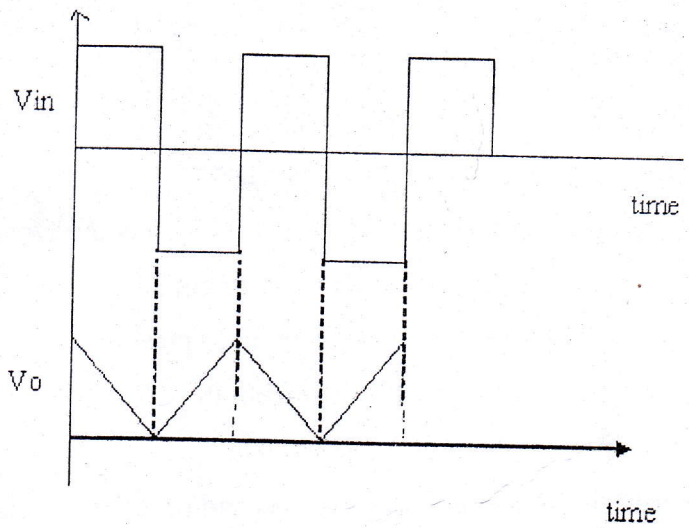
Thus the Inverting, Non-inverting amplifier, Integrator and Differentiator circuit was constructed and the output waveform was noted.

CIRCUIT DIAGRAM



Integrator

MODEL GRAPH



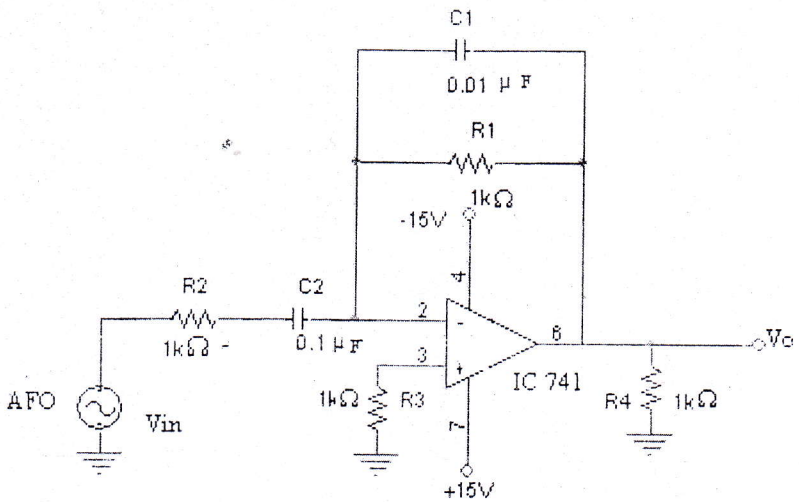
TABULATION

	Amplitude (Volts)	Time (ms)
Input		
Output		

REVIEW QUESTIONS

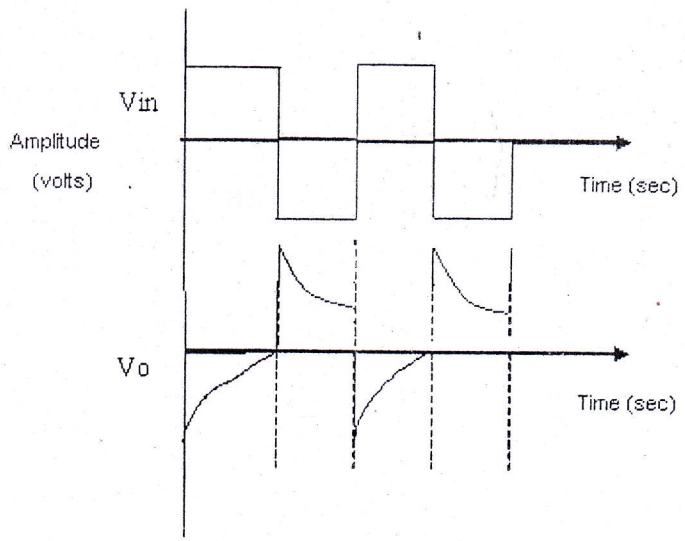
1. What is mean by Operational amplifier?
2. Mention the characteristics of an operational amplifier.
3. What is the gain formula for Inverting amplifier?
4. What kind of feedback is used in inverting amplifier?
5. What is the concept of virtual short in Op-Amp?

CIRCUIT DIAGRAM:



Differentiator

MODEL GRAPH



I/p & O/p waveforms

TABULATION

	Amplitude (volts)	Time (ms)
Input		
Output		

3. INSTRUMENTATION AMPLIFIER

AIM:

To Study the Operation of Instrumentation amplifier using IC 741.

APPRATUS REQUIRED:

S.No	COMPONENTS	RANGE	QUANTITY
1.	Op –amp	IC 741	1
2.	Resistor	22 KΩ	1
3.	Capacitor	0.1μf	1
4.	Connecting Wires		

THEORY:

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity light intensity etc. These physical quantities are measured with the help of transducer. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of instrumentation amplifier are high CMRR, low input impedance, high. Gain accuracy.

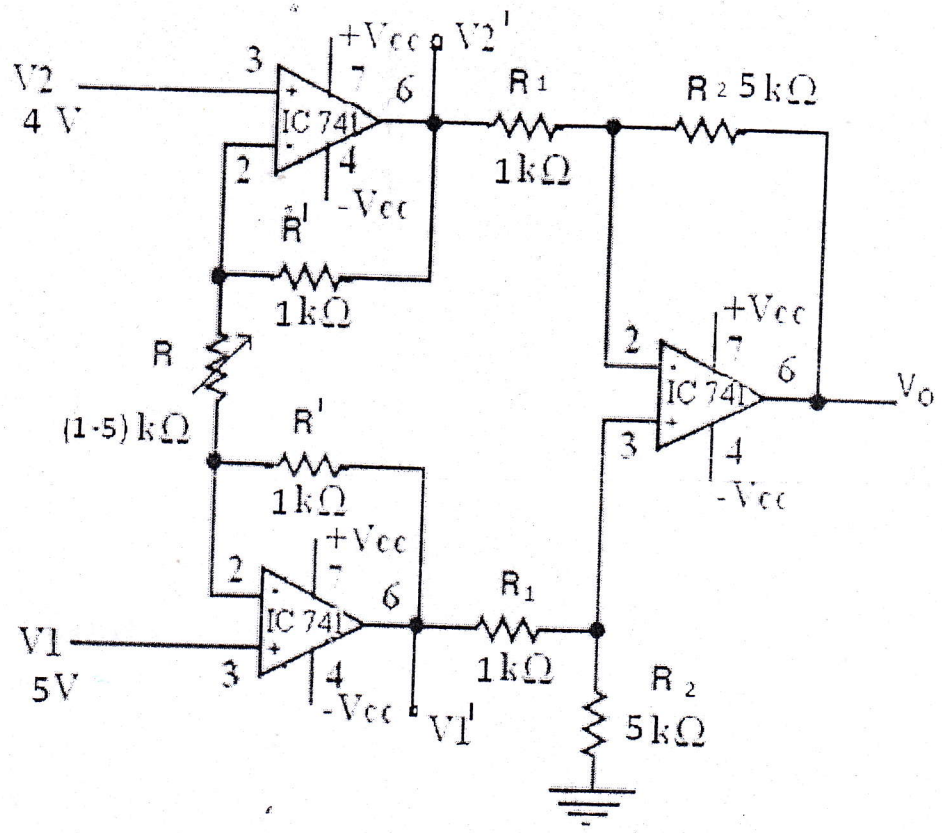
PROCEDURE:

1. Connections are made as per the Circuit diagram
2. Connect the dual supply voltage of +15V and -15V to bias the Operational amplifier.
3. In common mode an input of small voltage is applied as common to both the Operational amplifier.
4. In differential mode an input of different voltages are applied to both the Operational amplifier.
5. Amplitude and time period readings are tabulated.
6. Calculate the CMRR and Gain.

RESULT:

Thus the Instrumentation amplifier circuit was constructed and the output waveform was noted.

CIRCUIT DIAGRAM:



Instrumentation amplifier

TABULATION

R(KΩ)	V1'=(R'/R)(V1-V2)+V1	V2'=(-R'/R)(V1-V2)+V2	V0=(R2/R1)(V1'-V2

REVIEW QUESTIONS:

1. What is the need for an instrumentation Amplifier?
2. List the features of instrumentation Amplifier?
3. What are the applications of Instrumentation Amplifier?
4. Explain the difference between AC&DC Amplifier.
5. Draw a system whose gain is controllable by an adjustable resistance.

4. ACTIVE LOW PASS AND HIGH PASS FILTER

AIM:

To Design & Obtain the frequency response of a low pass and high pass filters having cutoff frequency 1 KHz and gain 3.

APPRATUS REQUIRED:

S.No	COMPONENTS	RANGE	QUANTITY
1.	Op –amp	IC 741	1
2.	Resistors	10KΩ, 20 KΩ,1.5 KΩ	1
3.	Capacitor	0.1μf	1
4.	Dual Power supply	0-30v	
5.	Cathode Ray Oscilloscope	(0-30)MHz	1
6.	Bread board		1

THEORY:

A filter is a circuit that is designed to pass a specified band of frequency while attenuating all the signals outside that band. Active filter circuits use the active elements such as op-amps, transistor along the resistors and capacitors. A low pass filter has a constant gain from 0 Hz to a high cutoff frequency. The frequency between 0Hz to f_{c2} are known as pass band frequencies where as the range of frequencies those beyond f_{c2} are attenuated.

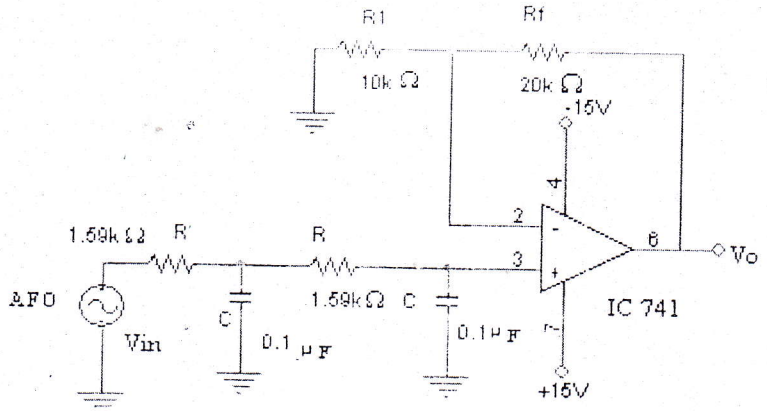
PROCEDURE:

1. Connections are made as per the Circuit diagram.
2. Connect the dual supply voltage of +15V and -15V to bias the Opamp.
3. A Sine wave is given as a input.
4. Vary the frequency, note down the corresponding output voltage.
5. The graph is drawn between the gain (y-axis) and the frequency (x-axis).

RESULT:

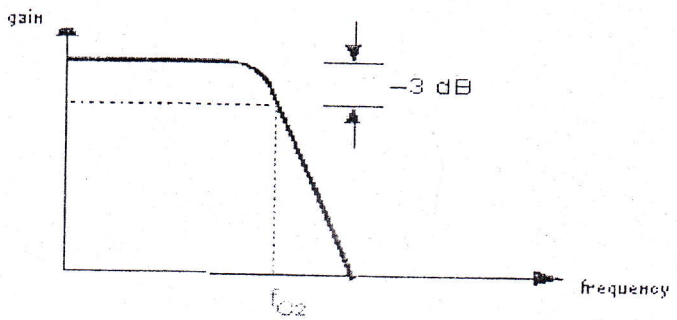
Thus the Low pass and high pass filter circuit was constructed and the output Waveform was noted.

CIRCUIT DIAGRAM:



LOW PASS FILTER

MODEL GRAPH



Low-pass filter

TABULATION

Frequency In Hz	Output Voltage(V_0)	V_0 / V_i	Gain = 20 log (V_0 / V_i)

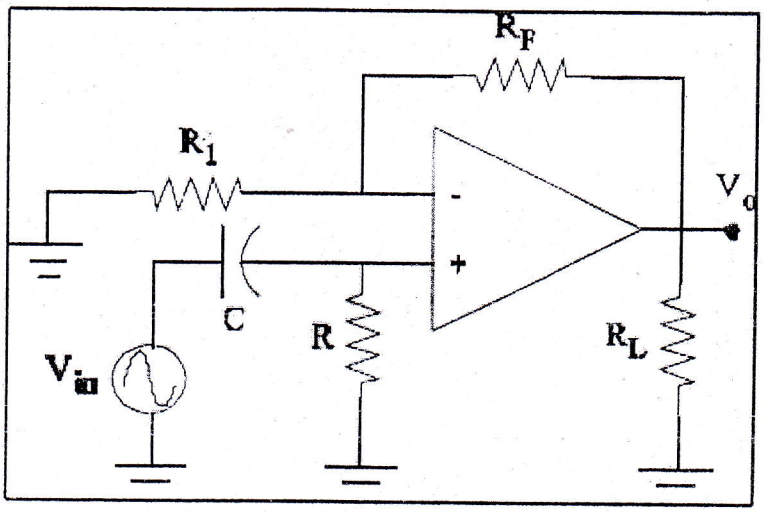
REVIEW QUESTIONS

1. What is a filter?
2. Define a notch filter?
3. What are the advantages of Active filters?
4. What are the demerits of passive filters?
5. Why do we use higher order filter?

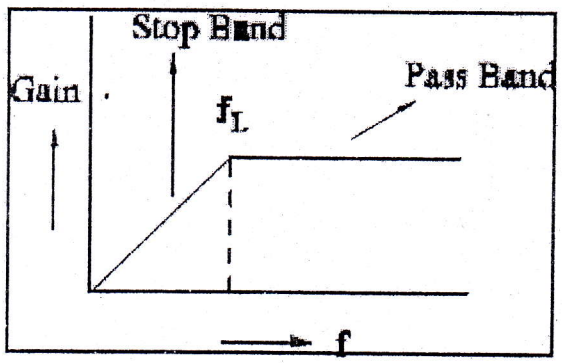
V_0 / V_i)

CIRCUIT DIAGRAM:

HIGH PASS FILTER



MODEL GRAPH



TABULATION

Frequency In Hz	Output Voltage(V_0)	V_0 / V_i	Gain = 20 log (V_0 / V_i)

5.ACTIVE NOTCH FILTER

AIM:

To design and setup a notch filter with a notch frequency f_N = 1 KHz.

APPRATUS REQUIRED:

S.No	COMPONENTS	RANGE	QUANTITY
1	Op-amp IC	μA741	2
2	Resistors	15KΩ,10KΩ,10KΩ,8.2KΩ	2,1
3	Capacitors	0.01μF, 0.02μF	2, 1
6	CRO	(0-20)MHz	1
4	Dual Power Supply	(15-0-15)V	1
5	Function Generator	(0-1)MHz	1
7	Bread Board		1

THEORY:

The narrow band reject filter is commonly called a notch filter and is useful for the rejection of single frequency. It is used to filter 60Hz power line frequency hum. The most commonly used notch filter is the *twin-T* network. This is a passive filter composed of two T-shaped networks. One T network is made up of two resistors and a capacitor, while the other uses two capacitors and a resistor. The notch-out frequency is the frequency at which maximum attenuation occurs; it is given by

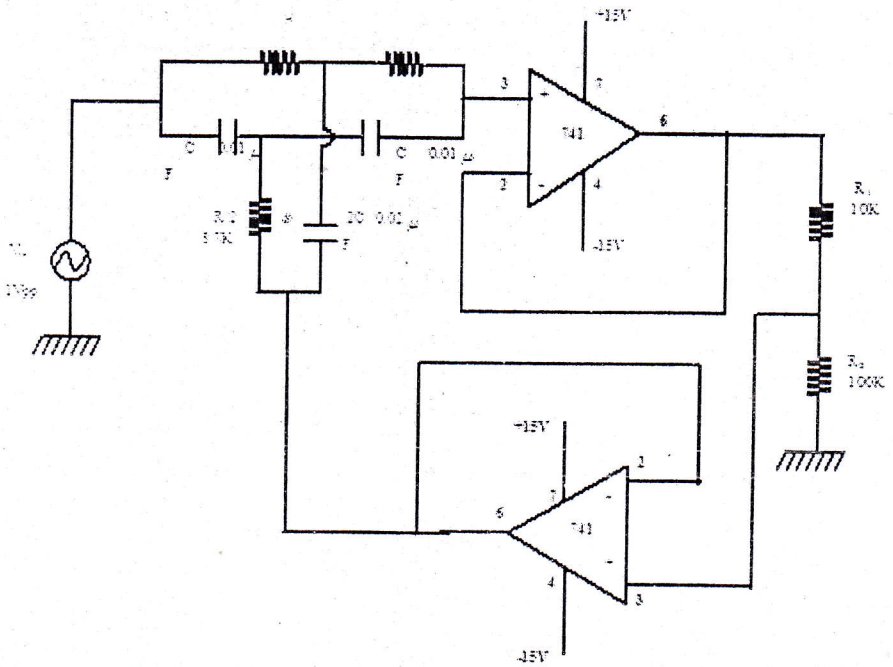
$$f_N = \frac{1}{2\pi RC}$$

PROCEDURE:

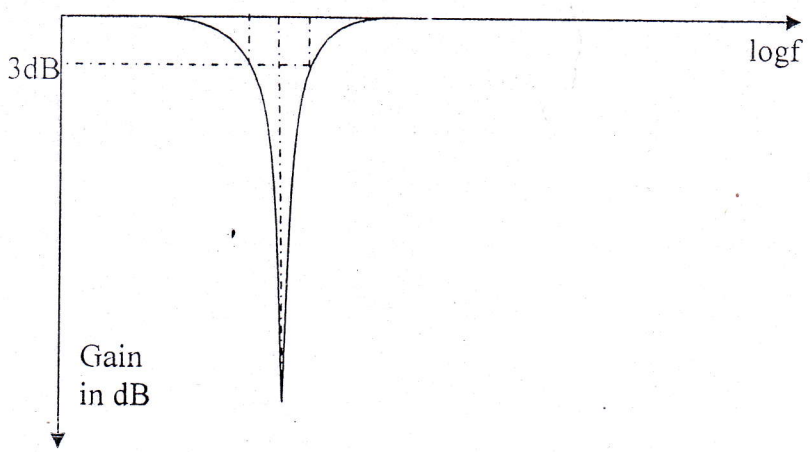
1. Set up the connections as shown in the circuit diagram on a bread board.
2. Connect the power supply to the circuit and switch ON.
3. Feed sine wave of $1V_{pp}$ to the input of the circuit.
4. Vary the input signal frequency of the circuit.
5. Measure the amplitude of the corresponding output wave from CRO.
6. Tabulate the readings.

in db
V_o/V_{in}

CIRCUIT DIAGRAM:



MODEL GRAPH



TABULATION

$V_{in} = 1V_{pp}$

F in Hz	Vo In volts	Log f	Gain in db $20\log V_o/V_{in}$

7. Plot the frequency response graph with log f along X-axis and gain along Y-axis.

RESULT:

Thus the active notch filter circuit was constructed and the output Waveform was noted.

6. WIENBRIDGE OSCILLATOR

AIM:

To study the operation of Weinbridge oscillator using IC741

APPRATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QUANTITY
1	Op-amp	IC741	1
2	Resistor	33k,12k,24k	1
3	Bread board		1
4	Dual power supply	0-30v	1
5	CRO	20MHZ	1

THEROY:

High-quality audio signal generators make extensive use of the Wien-Bridge oscillator as a basic building block. The feedback signal in this circuit is connected to the + ve input terminal .so that the opamp is working as a non inverting amplifier. Therefore the feedback network need not provide any phase shift. In this circuit a series RC network in one arm and a parallel RC network in adjoining arm. The condition of zero phase shifts around the circuit is achieved by balancing the bridge. The R-C network for frequency determination and a non-linear resistive network for amplitude stabilizations. The frequency of oscillation $f_0 = 1/2\prod RC$

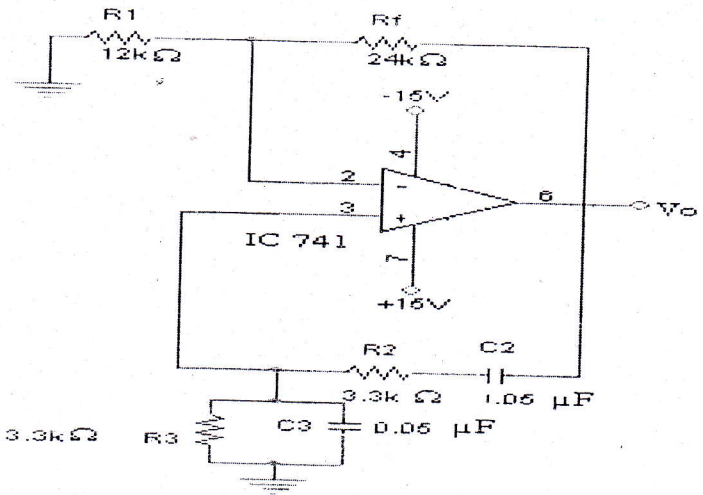
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Connect the dual supply voltage of -15v and +15v to op-amp
3. using the probes obtain the output from the CRO and compare with the input.
4. Tabulate the voltage and time period.
5. Plot the graph.

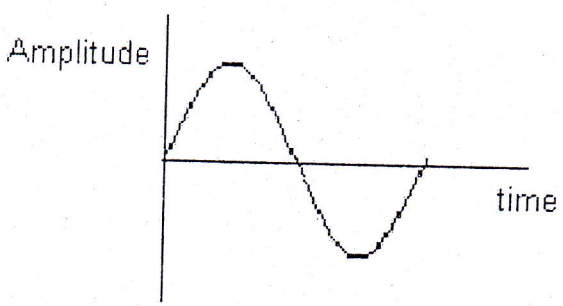
RESULT:

Thus the Wein bridge oscillator was constructed and the output waveforms have been studied.

CIRCUIT DIAGRAM



MODELGRAPH



TABULATION

	Amplitude	Time period
Input		
Output		

REVIEW QUESTIONS

1. What is barkhausen criterion?
2. How can you vary the frequency of oscillation in weinbridge oscillator?
3. What is the theoretical value of gain of the weinbridge oscillator
4. Why we need negative feedback in weinbridge oscillator.
5. What is the condition for sustained oscillation

7. PPM, PWM MODULATION AND DEMODULATION

AIM:

To generate PPM, PWM to observe the output waveform and also observe the demodulated output

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QUANTITY
1	Transistor	BC547	1
2	Function Generator		2
3	Resistor	1kΩ,75kΩ,2.2k Ω,i k Ω	Each 1
4	Capacitor	1Mf,10Mf,100Mf	Each 2
5	Probe		2
6	Bread Board		1
7	IC & Regulated Power Supply	+5V	1
8	CRO		1

THEORY:

In pulse position modulation, constant-width pulses are used, and the position or time of occurrence of each pulse from some reference time is made directly proportional to the amplitude of the information signal.

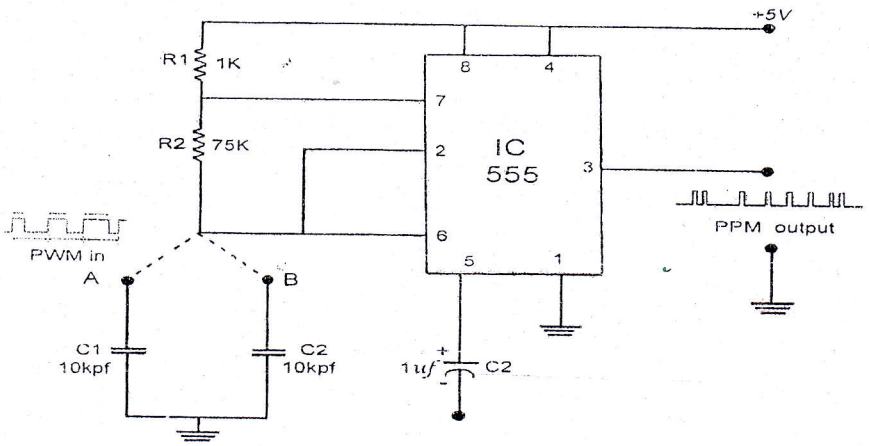
PROCEDURE:

MODULATION:

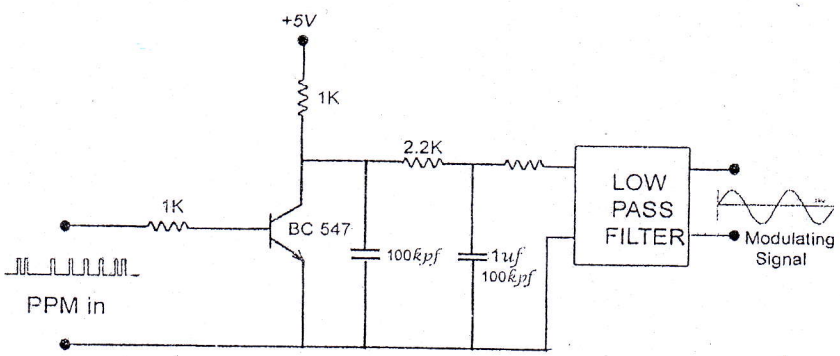
1. The circuit connections are given as per circuit diagram.
2. Before giving any input to the circuit the voltage and frequency of the output signal is measured which is the carrier signal.
3. The PWM wave is given as input from the function generator.
4. The output is observed and the position of the pulses in the modulated waveform is observed for 1 cycle.

CIRCUIT DIAGRAM:

PPM MODULATION



PPM DEMODULATION



TABULATION:

Modulating signal	Amplitude	Frequency
Carrier signal	Amplitude	Frequency
PPM signal	No. of pulses per cycle	
	Amplitude of pulses	

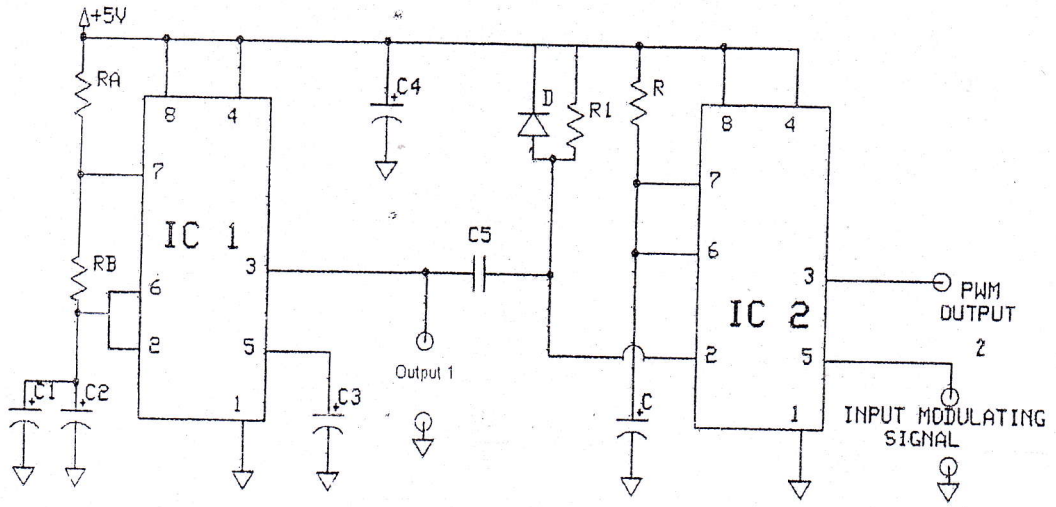
DEMODULATION:

1. The circuit connections are given as per circuit diagram.
2. The PPM output is given as input to the demodulator circuit
3. The frequency of the input signal is varied from 500Hz to 2 KHz.
4. The demodulated output is observed and is compared with the original modulating signal.

RESULT:

Thus the PPM, PWM wave was generated and the following was observed

CIRCUIT DIAGRAM:



IC_1 , IC_2 = Timer 555
R_A = 3.9 KΩ
R_B =3.3 KΩ
C_1 = C_2 = 0.01μf
C_3 =0.01μf
R =9.1Ω

TABULATION:

Modulating signal	Amplitude	Frequency
Carrier signal	Amplitude	Frequency
PWM signal	No. of pulses per cycle	
	Maximum width of pulses	
	Minimum width of pulses	
	Amplitude of pulses	

8. WAVEFORM GENERATORS –SQUARE, SAW-TOOTH AND TRIANGULAR WAVEFORMS

AIM:

To design a waveform generator to generate the waveforms like square waveform. saw tooth waveform and triangular waveform.

APPARATUS REQUIRED:

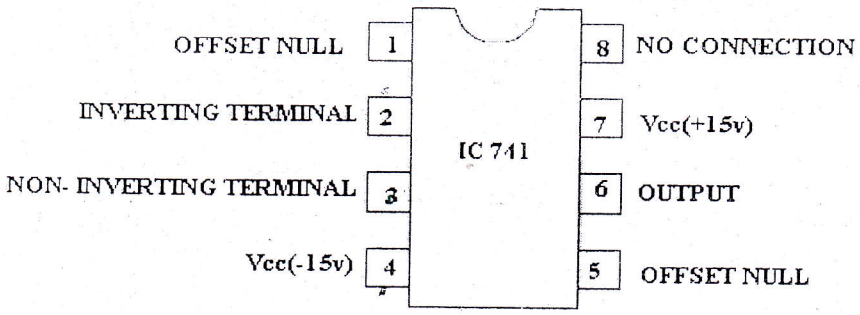
S.NO	COMPONENTS	RANGE	QUANTITY
1	IC 566	-	1
2	CRO	(0-30)MHz	1
3	RPS	(0-30)V	1
4	Function Generator	(0-30)MHz	1
5	Resistor	20kΩ	1
6	Capacitors	0.01μF 0.001μF	1
7	Bread Board	-	-
8	Connecting Wires	-	-

THEORY:

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage. The VCO provides the linear relationship between the applied voltage and the oscillation frequency. Applied voltage is called control voltage. The control of frequency with the help of control voltage is also called voltage to frequency converter.

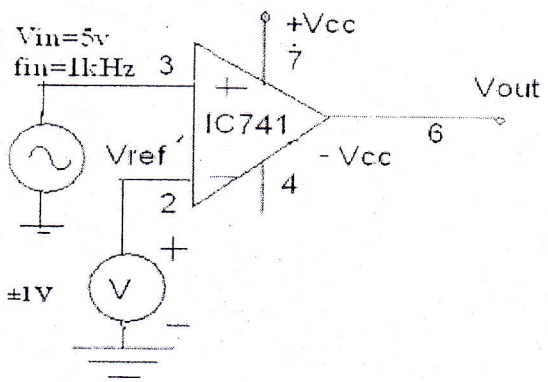
The commonly used VCO IC's are NE/SE 566, LM 566 etc.It is 8 pin IC, which provides two output pins. Its feature is that simultaneously IC provides square and triangular wave outputs which are the functions of input voltage. The input voltage is also called as Modulating input voltage.

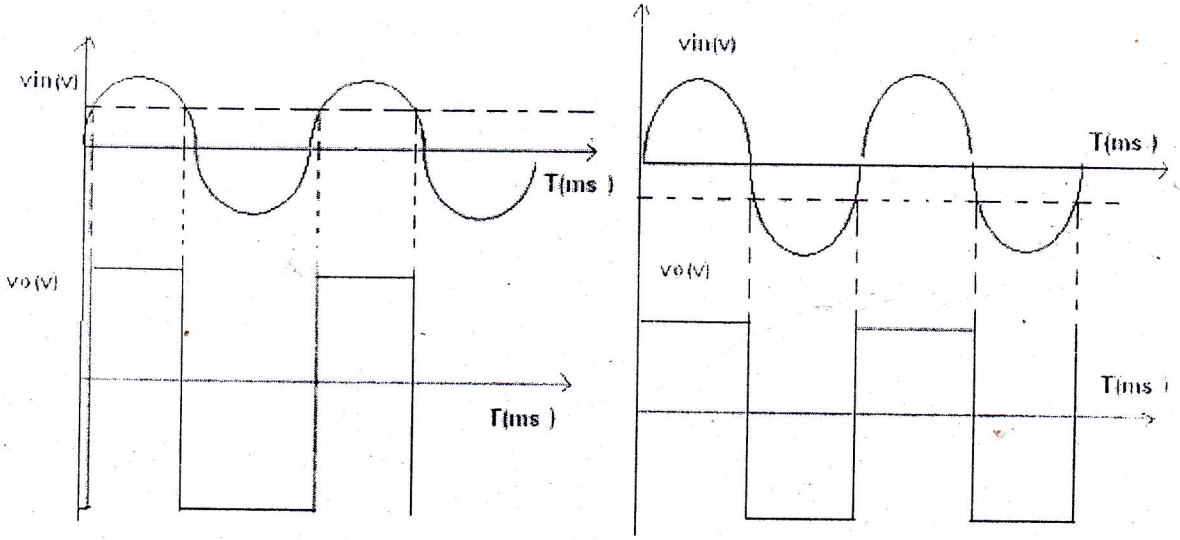
PIN DIAGRAM:



CIRCUIT DIAGRAM:

NON INVERTING COMPARATOR





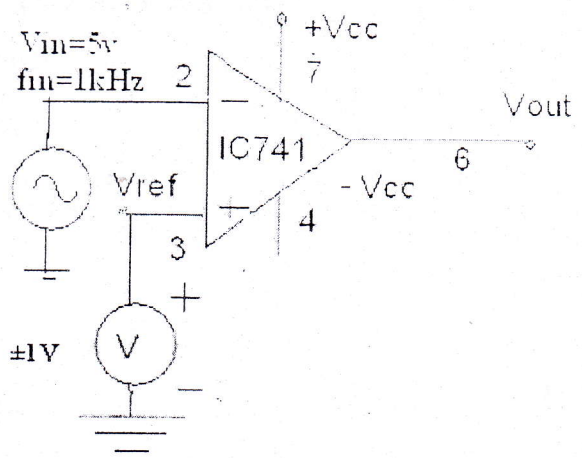
PROCEDURE:

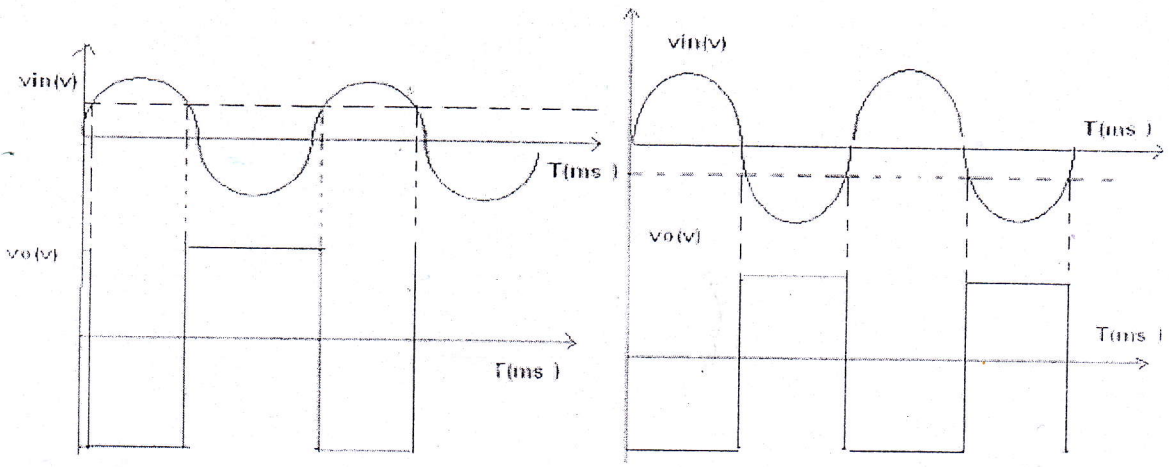
1. Connections are given as per the circuit diagram.
2. Connect +10V to pin-8 and the modulating input is given to the pin-5.
3. Connect the output channel of CRO to the pin-4 to observe the triangular output.
4. And the next channel of CRO is connected to the pin-3 to observe the square wave output.

RESULT:

Thus the various waveforms like square, saw-tooth and triangular waveforms are generated .

INVERTING COMPARATOR:





TABULATION:

INPUT VOLTAGEVIN(V)= 5v,1KHz(sin)

Vref	AMPLITUDE(V)	T0N(ms)	TOFF(ms)	T(ms)
	INVERTING COMPARATOR			
	NON- INVERTING COMPARATOR			

9. ASTABLE MULTIVIBRATOR USING OPAMP

AIM:

To design an Astable multivibrator using IC 741.

APPRATUS REQUIRED:

S.No	COMPONENTS	RANGE	QUANTITY
1.	Op –amp	IC 741	1
2.	Resistors	10KΩ,20 KΩ,1.5 KΩ,	1
3.	Capacitor	0.1μf	1
4.	Dual Power supply	0-30v	
5.	Function Generator	(0-3)MHz	1
5.	Cathode Ray Oscilloscope	(0-30)MHz	1
6.	Bread board		1
7..	Connecting Wires		

THEROY:

A simple Opamp squrewave generator is also called as free running oscillator. The principle of generation of square wave output is to force an opamp to operate in saturation region. A fraction $\beta=R_2/(R_1+R_2)$ of the output is feedback to the + input terminal. The output is also feedback to the –ve input terminal after integrating by means of of a low pass RC combination. Whenever the input at the –ve terminal exceeds Vref, switching takes place resulting in a square wave output. The circuit has two quasistable states (no stable states).Thus, there is oscillation between these two states and no external signals are required to produce the change in state.

Total time period is given as $T=2RC \ln(1+\beta)/(1-\beta)$.

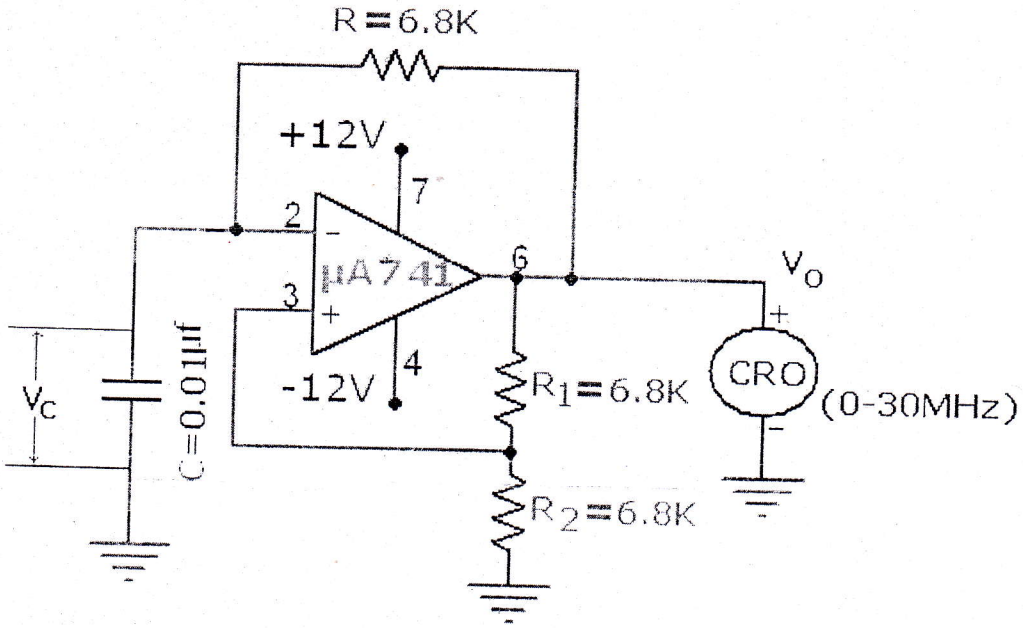
If $R_1=R_2$ $\beta=0.5$ Then $T=2RC\ln 3$

If $R_1=1.16R_2$ Then $T=2RC$ $F_0=1/2RC$

Monostable Multivibrator:

In monostable multivibrator the diode D_1 is connected across the capacitor(C). The diode clamps the capacitor voltage to 0.7V. When the output is at $+V_{sat}$, narrow negative triggering pulse V_t is applied to non inverting terminal through diode D_2. Let us assume the output voltage V_O is at $+V_{sat}$ in its stable state. The diode D_1 conducts and the voltage across the capacitor(C) is V_C gets clamped to 0.7V. The voltage at non inverting input terminal is controlled by potentiometer divides of R_1R_2 to βV_O. i.e. $+\beta V_{sat}$ in stable

Circuit Diagram for Astable Multivibrator Using Op-amp:



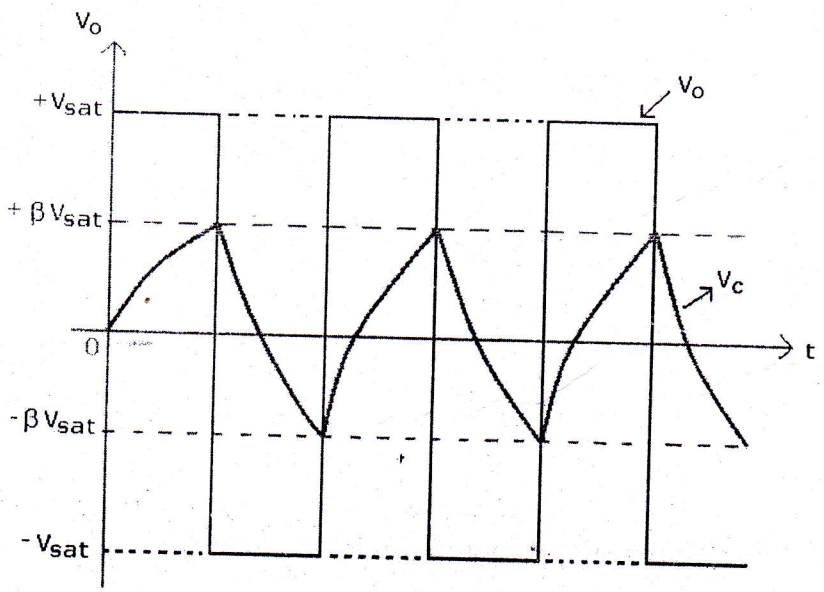
Astable Multivibrator using Op-amp

Design:

$$R_1 = R_2 = R = 6.8K\Omega \quad C = 0.01\mu f \quad \beta = \frac{R_2}{R_1 + R_2} = 0.5$$

$$T = 2RC \ln\left[\frac{1+\beta}{1-\beta}\right] = 0.15ms \qquad \text{Frequency}(f) = \frac{1}{T} = 6.7KHz$$

Model Graph:



Waveforms of Astable Multivibrator

state. If V_t is a negative trigger of amplitude so that effective voltage at this terminal is less than 0.7V (+ β V_{sat} + (-V_t) then the output of the op-amp changes its state from + V_{sat} to -V_{sat}. The diode is now reverse biased and the capacitor starts charging exponentially to -V_{sat} through resistance R. The time constant of charging is zero.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Connect the dual supply voltage of -15v and +15v to op-amp
3. A sine wave of 1VPP at 2 KHz is given as input to pin2.
4. using the probes obtain the output from the CRO and compare with the input.
5. Tabulate the voltage and time period.
6. Plot the graph.

RESULT:

Thus the A stable and Monostable multivibrator using IC 741 was constructed and the output waveforms have been studied.

REVIEW QUESTIONS

1. What is a mutivibrator?
2. What is the use of a stable multivibrator?
3. How many stable states are available in a stable multivibrator?
4. What is the use of Zener diode in a stable multivibrator?
5. What is the other name of astable multivibrator?

Tabulation:

Astable Multivibrator

S.NO	Capacitor Voltage (V_C) in volts	Time in ms	Output Voltage (V_O) in volts	Time in ms

Monostable Multivibrator

S.NO	Input Voltage (V_i) in volts	Output Voltage (V_O) in volts	Time in ms	
			T_{ON}	T_{OFF}

11. 723 VOLTAGE REGULATOR

AIM:

To study the operation of 723 Regulator IC.

APPARATUS REQUIRED:

S.NO	APPARATUS	TYPE/RANGE	QUANTITY
1.	RPS	(0-30)v	1
2.	Regulator	IC 723	1
3.	Resistor	680Ω,10kΩ,2.2kΩ, 33Ω, 1kΩ	1,2
4.	Capacitor	100pF	1
5.	Breadboard	-	1
6.	Connecting wires	-	Required
7.	Ammeter	(0-30mA)	1

THEORY:

The IC 723 voltage regulator overcomes the limitations of three terminal regulators such as no short circuit protection and output voltage (positive or negative) is fixed. The IC 723 is adjustable over a wide range of both positive or negative voltage is regulated. This IC is inherently low current device, but can boost to provide 5 amps or more current by connection of 723 is that it has no in – inbuilt thermal protection.

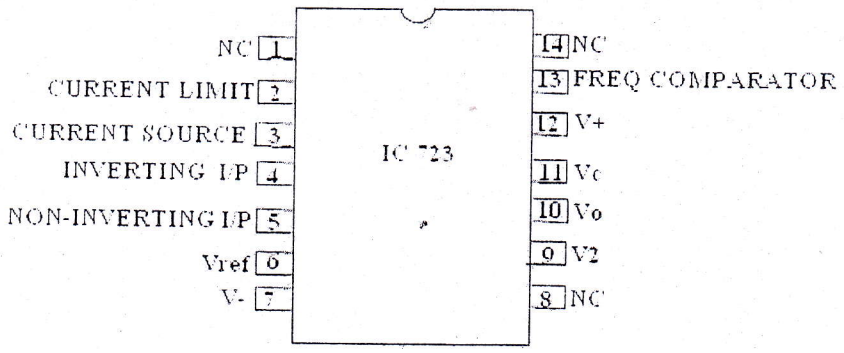
The voltage at the NI terminal of the amplifier due to R1R2 divider is Vin= Vref (R2/R1+R2).the difference between Vin and the output voltage Vo which is directly fed back to the inv terminal is amplifier by the error amplifier. The output of the error amplifier devices the pass transistor Q, as to make the amplifier are minimum VO=Vref (R2/R1+R2).

If the output voltage becomes low, the voltage at Inv terminal of error amplifier goes down. This makes the output of error amplifier to become more positive .the voltage across load increases. This IC is provided with a current limit facility. The current limit is set by connecting an external resistance Rsc between the terminal Cl and Cs terminals together. The Cl terminal is also connected to the output terminal Vo and Cs to the load terminal.

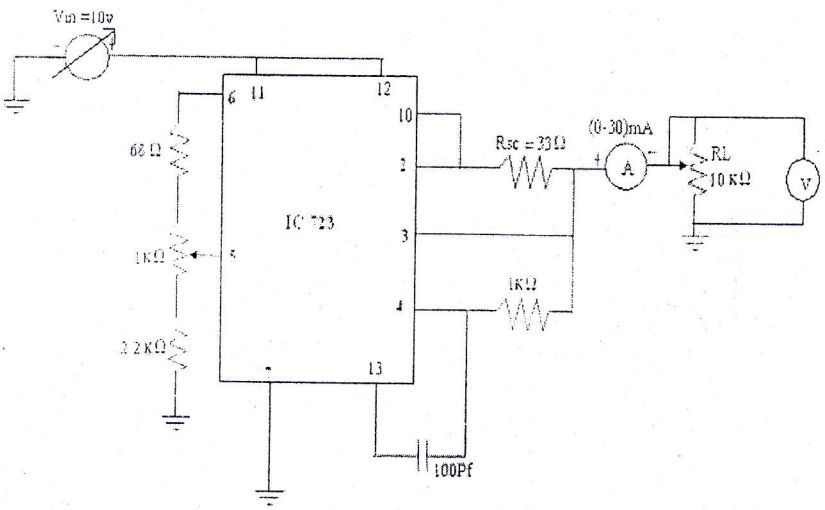
PROCEDURE:

1. Set the dc power supply, Vin=10v
2. Measure & record Vref

PIN DIAGRAM:



CIRCUIT DIAGRAM:



TABULATION:

LINE REGULATION:

IL=0.5 mA

Vi (v)	VL (v)

1. Remove RL & measure the minimum and maximum output voltage between the wiper arm of the 1kΩ and ground.
2. Adjust the 1kΩ so that VO=5v and measure the voltage between wiper arm of the 1kΩ and ground.
3. Adjust RL until IL=1mA and note VI for various values of I2, note Vl and calculate load regulation.
4. Gradually increase IL above 18mA, VL decreases, when IL is about 18 to 20 mA. Measure Il and Vl for below and above the current limiting point.
5. Plot the graph IL vs. VL.
6. Replace Rl with short circuit currents Isc.
7. Make Rsc=0, with VIN =10V.
8. Adjust Rl for IC of 1mA .determine the line regulation and measure and record VL for various values of input voltage and percentage line regulation.

RESULT:

Thus the operation of 723 voltage regulator was studied and the line and load regulations are found and plotted in the graph.

LOAD REGULATION

R(KΩ) VL(V) IL(mA)		

REVIEW QUESTIONS

1. What is a voltage regulator ?

2. Define load regulation.

3 Define line regulation.

4. Give the draw back of linear regulator.

5. What are the advantages of IC Voltage regulator.

12. ADC/DAC USING OP-AMP

AIM:

To rig up circuit to convert an analog voltage to its digital equivalent (ADC), and from digital to analog voltage conversion (DAC)

APPARATUS REQUIRED:

S. NO	COMPONENTS	RANGE	QUANTITY
1	Power Supply	(0-30)V	1
2	Operational Amplifier	LM 324,IC 741	2
3	Resistor	10KΩ,100KΩ,1KΩ,8.2KΩ	4,1,6,1
4	Capacitors	0.1μF,0.01 μF	1,2
5	NAND Gate	IC 7400	1
6	Multimeter	-	1
7	Bread Board	-	1
8	Connecting Wires	-	As Required

THEORY:

A DAC accepts an n-bit input word b1, b2, b3... bn in binary and produce an analog signal proportional to it. Each digital input requires an electrical signal, representing either a logic 1 or a logic 0.

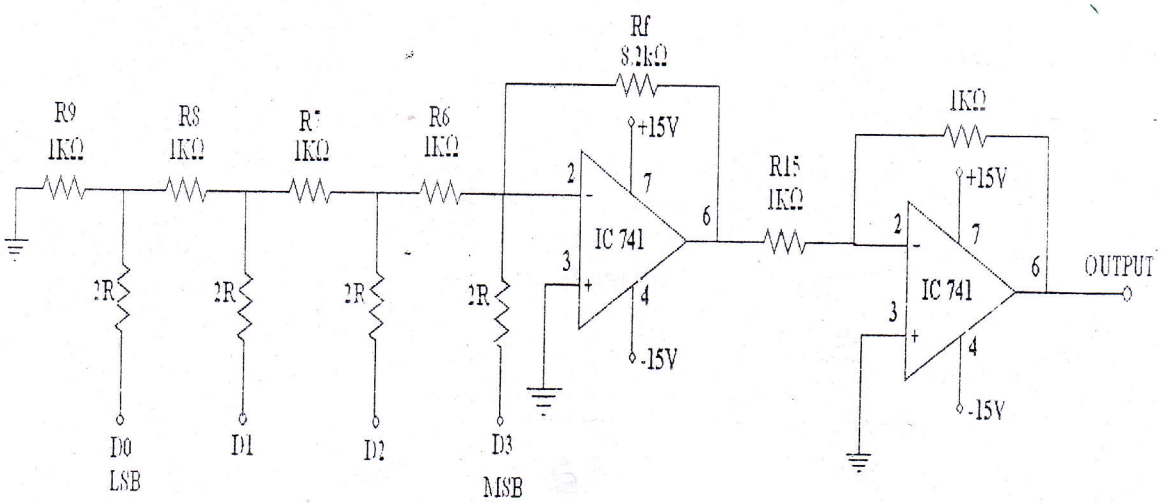
Basic conversion techniques:

1. Binary.weighted resistor D/A converter
2. R/2R ladder D/A converter

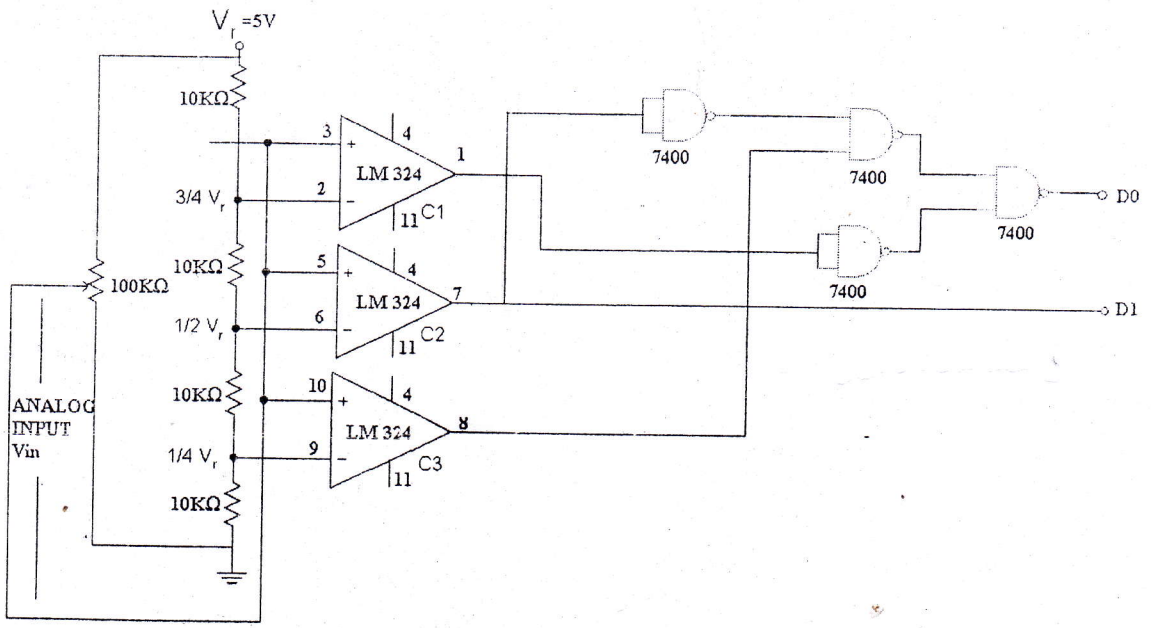
In these techniques the shunt resistors are used to generate n binary weighted currents.These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called current driven DAC's.

CIRCUIT DIAGRAM:

DIGITAL TO ANALOG CONVERTER:



ANALOG TO DIGITAL CONVERTER:



R/2R ladder D/A converter uses only two resistor values. This avoids resistance spread drawback of binary weighted D/A converter. R/2R ladder D/A converter uses shunt resistors to generate n binary weighted currents. However it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC. Voltage scaling requires an additional set of voltage dropping series resistances between adjacent nodes.

ANALOG TO DIGITAL CONVERTER:

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function that of the D/A converter.

Analog to Digital converter are classified into two general groups based on the conversion techniques. One technique involves comparing a given analog signal with the internally generated reference voltages. This group includes successive approximation, flash, delta modulated, adaptive delta modulated and flash type converters. Another technique involves changing an analog signal into time or frequency and comparing these two parameters against known values.

Flash A/D converters, also known as a simultaneous or parallel comparator ADC, because the fast conversion speed is accomplished by providing 2^n-1 comparators and simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

The comparators give the output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referred above the input signal, remain turned-off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The coding resulting from this comparator is converted to a binary code by the encoder.

TABULATION:

DIGITAL TO ANALOG CONVERTER:

INPUTS				OUTPUTS	
B3	B2	B1	B0	PRACTICAL	THEORETICAL
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

ANALOG TO DIGITAL CONVERTER:

ANALOG INPUT VIN	C3	C2	C1	D1	D0
0 to V/4	0	0	0	0	0
V/4 to V/2	0	0	1	0	1
V/2 to 3V/4	0	1	1	1	0
3V/4 to V	1	1	1	1	1

PROCEDURE:

DIGITAL TO ANALOG CONVERTER:

1. Connect the circuit as per the circuit diagram
2. Connect V+ (pin 7) terminal of the OPAMP to +5V
3. Connect V- (pin4) terminal of the OPAMP to g-5V
4. Verify the analog output for different digital values..

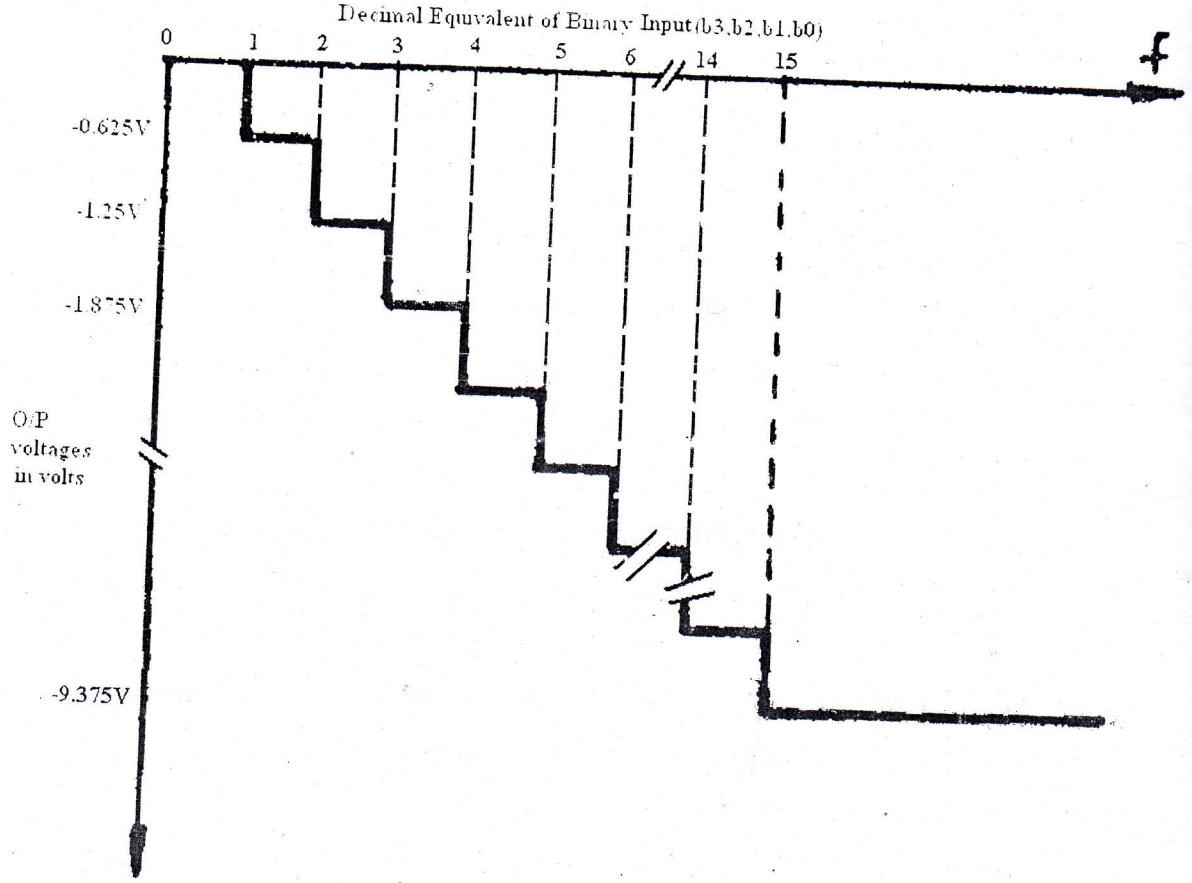
ANALOG TO DIGITAL CONVERTER:

1. Connect the circuit as per the circuit diagram
2. Connect V+ (pin 4) terminal of the OPAMP to +5v
3. Connect V- (pin11) terminal of the OPAMP to ground
4. Verify the digital output for different analog voltages

RESULT:

Thus the DAC and the ADC circuit are constructed and outputs are observed.

MODEL GRAPH:


Decimal Equivalent of Binary Input(b3,b2,b1,b0)
0
1
2
3
4
5
6
14
15
-0.625V
-1.25V
-1.875V
O/P voltages in volts
-9.375V

13. PLL CHARACTERISTICS AND FREQUENCY MULTIPLIER USING PLL

AIM:

To construct and study the operation of PLL IC 565 and determine its Characteristics.

APPARATUS REQUIRED:

S.NO	COMPONENTS	RANGE	QUANTITY
1	IC 565	-	1
2	Resistors	6.8 KΩ,4.7KΩ,2KΩ	1
3	Capacitors	0.001μF,0.1μF,1μF,0.01μF,10μF	1
4	Function Generator	2 MHz	1
5	C.R.O	-	1
6	Dual Power Supply	(0- 30) V	1

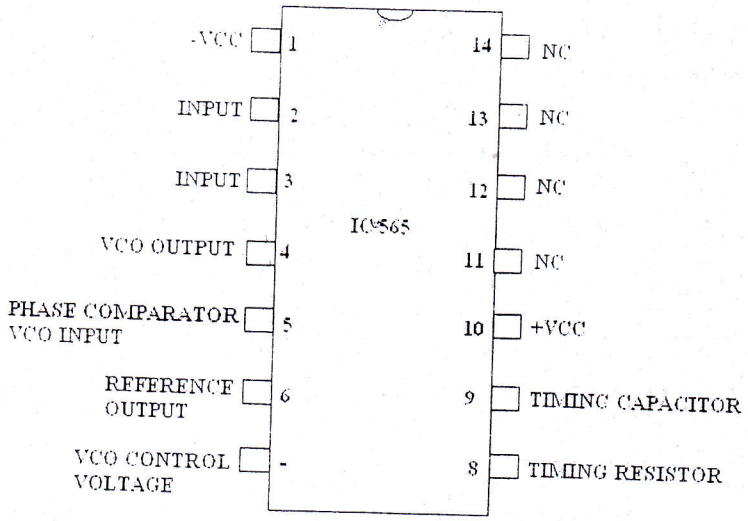
THEORY:

A Phase locked loop is basically a closed loop system designed to lock the output frequency and phase to the frequency and phase of an input signal. The phase locked loop consists of,

- Phase detector
- Low pass filter
- Error amplifier
- Voltage controlled Oscillator

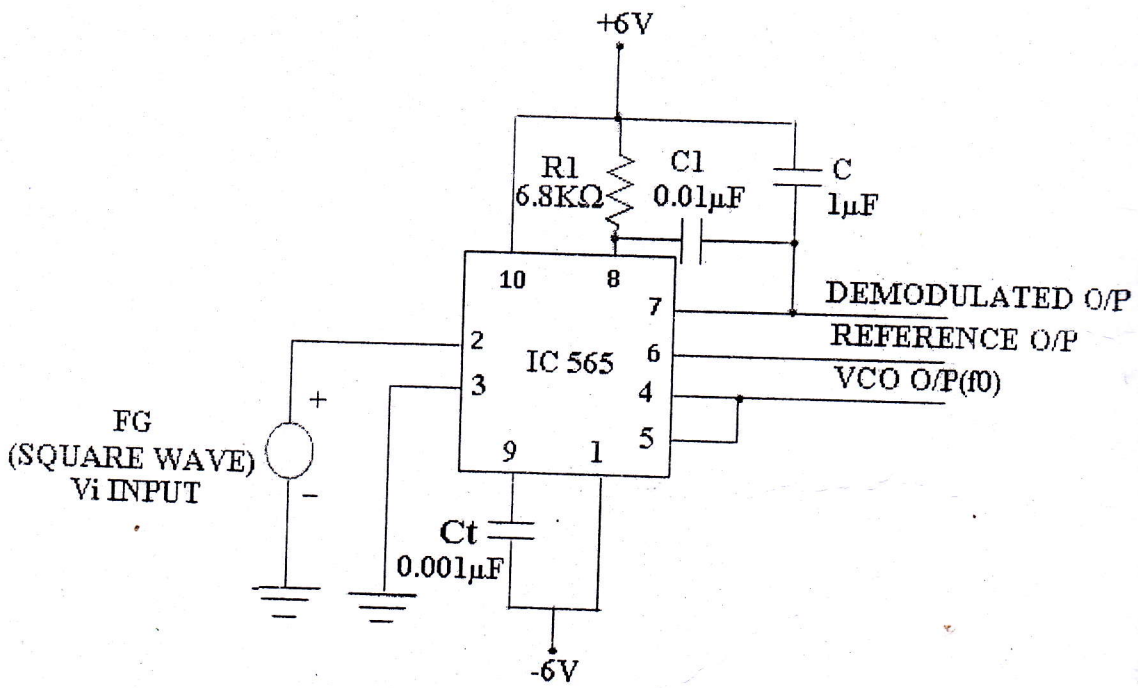
PLL 565 is used for the frequency multiplier. A divide by N network is inserted between the VCO output (pin-4) and the phase comparator input (pin-5).Since the output of the divider is locked to the input frequency f_i ,the VCO is actually running at a multiple of running frequency. By selecting proper divider by N network, we can obtain desired multiplication. The IC 7490 is a 4 bit binary counter. It is configured as a divide by 10 circuit.

PIN DIAGRAM (IC 565 - PLL):



CIRCUIT DIAGRAM:

PLL CHARACTERISTICS:



TABULATION:

PLL CHARACTERISTICS:

S.NO	INPUT FREQUENCY(Hz)	AMPLITUDE(V)	TIME PERIOD(mS)	OUTPUT FREQUENCY

FREQUENCY MULTIPLIER USING PLL:

TABULATION:

S.NO	AMPLITUDE(V)	TIME PERIOD(MS)	FREQUENCY(HZ)

FREQUENCY MULTIPLIER USING PLL:

1. The connections are given as per the circuit diagram.
2. The circuit uses a 4- bit binary counter 7490 used as a divide-by-5 circuit.
3. Measure the free running frequency of VCO at pin 4, with the input signal V_i set equal to zero. Compare it with the calculated value = $0.25 / (R_T C_T)$.
4. Now apply the input signal of 1 V_{PP} square wave at 500 Hz to pin 2.
5. Vary the VCO frequency by adjusting the 20kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
6. Repeat steps 4,5 for input frequency of 1 kHz and 1.5 kHz.

RESULT:

Thus the PLL circuit and the frequency multiplier circuit is constructed and its Characteristics is determined.

PROCEDURE:

PLL CHARACTERISTICS:

1. The connections are given as per the circuit diagram.
2. Measure the free running frequency of VCO at pin 4, with the input signal V_i set equal to zero. Compare it with the calculated value = $0.25 / (R_T C_T)$.
3. Now apply the input signal of 1 V_{PP} square wave at a 1 KHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.
4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f1 gives the lower end of the capture range. Go on increasing the input frequency, till Pll tracks the input signal, say ,to a frequency f2.This frequency f2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f3,the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f4 gives the lower end of the lock range.
6. The lock range $\Delta f_L = (f2 - f4)$.Compare it with the calculated value

Of $\pm$ 7.8 fo / 12 .Also the capture range is $\Delta f_c = (f3 - f1)$.Compare it with the calculated value of capture range.

$$\Delta f_c = \pm (\Delta f_L / (2\pi)(3.6)(10^3) C)^{1/2}$$

REVIEW QUESTIONS

1. Mention some areas where PLL is widely used?
2. List the basic building block of PLL.
3. Define lock in range of PLL.
4. Define capture range of PLL.
5. Define Pull-in time

14. ASTABLE MULTIVIBRATOR USING IC555

AIM:

To design Astable multivibrator using IC555.

APPRATUS REQUIRED

S.NO	COMPONENTS	RANGE	QUANTITY
1	IC555	NE555	1
2	Resistor	22KΩ	2
3	Bread board		1
4	Dual power supply	0-30v	1
5	Cathode ray oscilloscope	20MHZ	1

THEORY:

Astable multivibrator has no stable state. Astable multivibrator changes its state alternatively. Hence the operation is also called free running non-sinusoidal oscillator. A stable circuit used to obtain square wave output. The important application of astable multivibrator is voltage controlled oscillator. In a stable multivibrator is a timing circuit whose 'low' and 'high' states are both unstable. As such, the output of an a stable multivibrator toggles between 'low' and 'high' continuously, in effect generating a train of pulses. This circuit is therefore also known as a 'pulse generator' circuit.

The charging time is given by $T1=0.69(Ra+Rb)C$

The discharge time is given by: $T2=0.69Rb\ C$

The total period can therefore be expressed as: $T=.69(Ra+Rb)C$

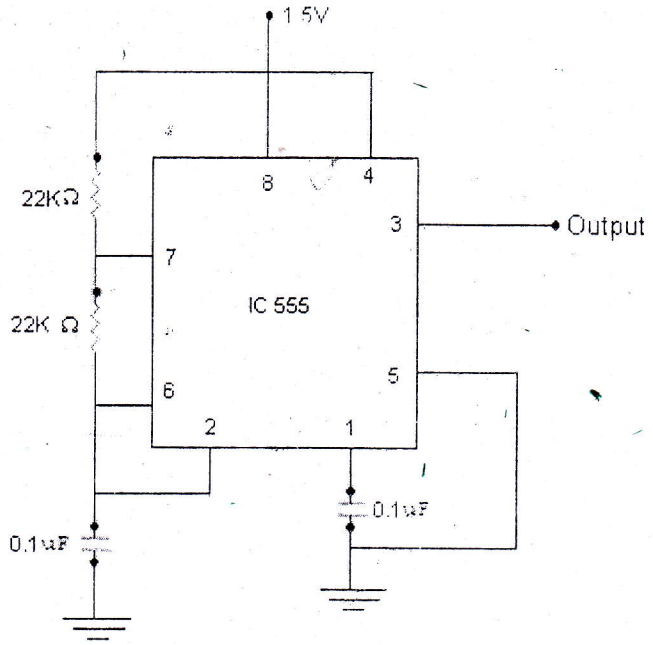
The duty cycle can be derived from T1 and T2 as:

Duty Cycle = $(Ra + Rb)/(Ra + 2Rb)$

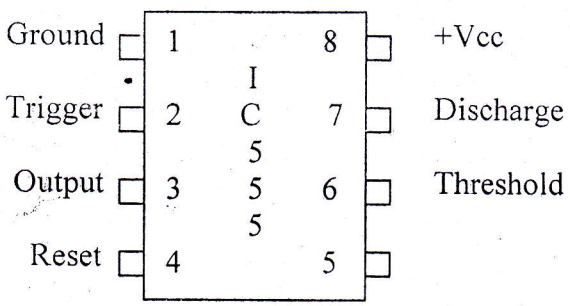
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Connect the dual supply voltage of -15v and +15v to op-amp
3. using the probes obtain the output from the CRO and compare with the input.

CIRCUIT DIAGRAM



PIN DETAILS



TABULATION

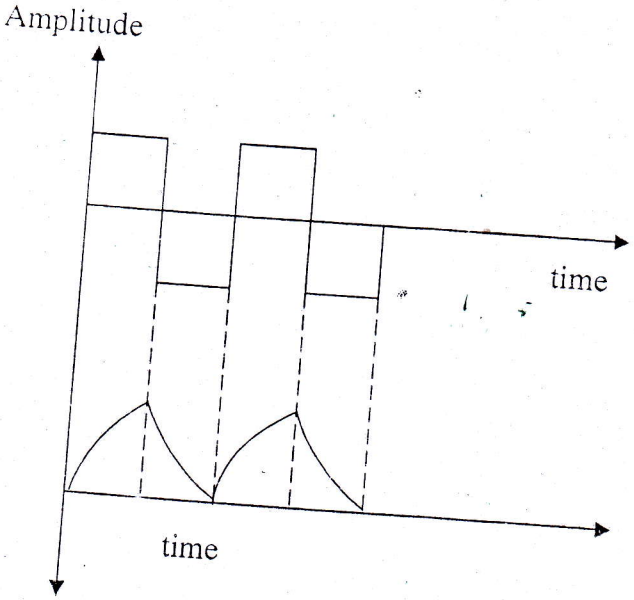
Type	Amplitude	Time period
Square Wave		
Spike Wave		

4. Tabulate the voltage and time period.
5. Plot the graph.

RESULT:

Thus the Astable multivibrator was constructed and the output waveforms have been studied.

MODEL GRAPH



REVIEW QUESTIONS

1. What are the modes of operation of timer?
2. Define Duty cycle.
3. Explain the function of reset.
4. How is an Astable multivibrator connected in to a pulse position modulator?
5. Give any four applications of Astablemode.

15. A MONOSTABLE MULTIVIBRATOR USING IC555

AIM:

To design a Monostable multivibrator using IC 741.

APPRATUS REQUIRED:

S.NO	Name of the components	Range/Type	Quantity
1	IC	IC 555	1
2	Resistor	10K	1
3	Capacitor	1μF	1
4	CRO	30MHz	1
5	Connecting Wires	-	-

THEORY:

Monostable multivibraor has one stable state and one quasi-stable state. So is also called as one shot multivibraor. This circuit is useful for generating single output pulse of adjustable time duration. It can be made to switch to another state by the application of triggering pulse. It returns to its stable sate after a time interval determined by circuit component value.

$T=R\ C\ \ln [1+R2/R1]$

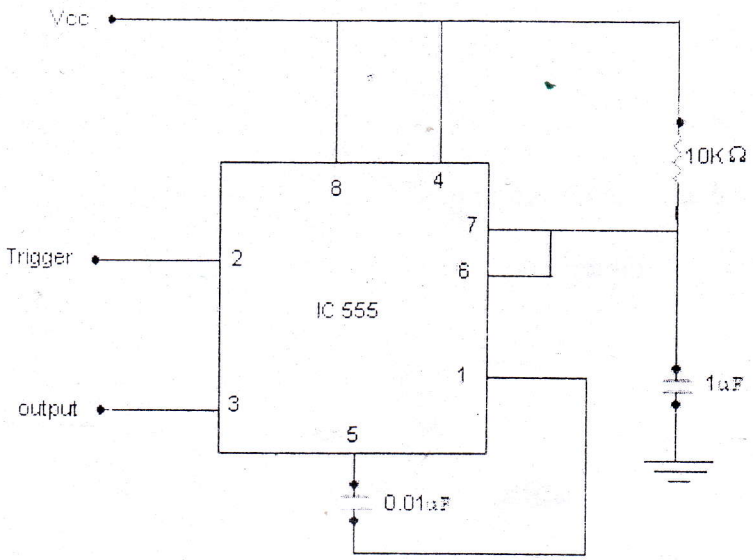
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Input trigger pulse is given to the circuit.
3. Notice the corresponding output at the CRO.
3. Plot the waveforms.

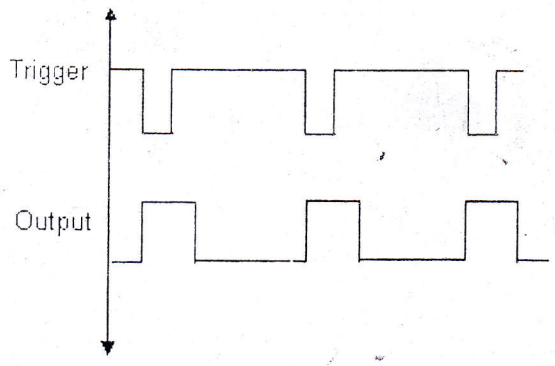
RESULT:

Thus the Monostable multivibrator was constructed and the output waveforms have been studied.

CIRCUIT DIAGRAM



MODELGRAPH



TABULATION:

Type	Amplitude in volts	Time period in ms
Input		
Output		

REVIEW QUESTIONS

1. List any four applications of 555 timers in monostable mode of operation.
2. What is frequency divider?
3. What is the function of missing pulse detector?
4. Derive the expression of time delay of a monostable multivibrator.
5. Give some methods for obtaining symmetrical square waveform.