AVIT
AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY

VINAYAKA MISSION'S RESEARCH FOUNDATION
(Deemed to be University under section 3 of the UGC Act 1956)

Accredited by NAAC

Approved by AICTE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Lab Manuals

DEPARTMENT	**: ECE**
NAME OF THE SUBJECT	**: SEMICONDUCTOR DEVICES**
Subject Code	**: 17ECCC81**
REGULATION	**: R2017**

HOD/ ECE

17ECCC81	SEMICONDUCTOR DEVICESLAB	Category	L	T	P	Credit
		CC	0	0	4	2

PREAMBLE

To reinforce learning in the accompanying semiconductor devices course through hands-on experience by examining the electrical characteristics of various semiconductor devices, such as diodes, BJTs and FETs. To provide the student with the capability for performing various analysis of semiconductor devices.

PRERQUISITE- NIL

COURSE OBJECTIVES

1	To emphasize the practical, hands-on component of this course.
2	To complementthe theoretical material presented in lecture, and as such, is integral and indispensible to the mastery of the subject.
3	To study experimentally the characteristics of diodes, BJT's and FET's.
4	To verify practically the response of various special purpose electron devices.
5	To provide students engineering skills by way of breadboard circuit design with electronic devicesand components.

COURSE OUTCOMES

On the successful completion of the course, students will be able to

CO1. Construct and find the ripple factor and efficiency of HWR and FWR by conducting experiments.	Apply
CO2. Construct clipper and clamper circuits for any given specifications and illustrate their output.	Apply
CO3. Determine the given transistor parameters from the characteristics of BJT in CE and CC Configuration.	Apply
CO4. Design transistor voltage regulator for given specifications and verify its output.	Analyze
CO5. Examine the characteristics of SCR, DIAC and TRIAC.	Analyze

MAPPING WITH PROGRAMME OUTCOMES AND PROGRAMME SPECIFIC OUTCOMES

COS	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO2	PSO3
CO1	S	M	M	-	-	-	M	-	M	-	M	-	S	M	-
CO2	S	M	M	-	-	-	M	-	M	-	M	-	S	M	-
CO3	S	M	M	-	-	-	M	-	M	-	M	-	S	M	-
CO4	S	M	M	-	-	-	M	-	M	-	M	-	S	M	M
CO5	S	M	M	-	-	-	M	-	M	-	M	-	S	M	-

S- Strong; M-Medium; L-Low

LIST OF EXPERIMENTS

1. Half Wave Rectifier
2. Full Wave Rectifier
3. Clipper
4. Clamper
5. Input/output Characteristics of CE Amplifier
6. Input/output Characteristics of CC Amplifier
7. Transfer Characteristics of JFET
8. Voltage Regulator
9. TRIAC, DIAC
10. SCR

COURSE DESIGNERS

S.No.	Name of the Faculty	Designation	Department	Mail ID
1	Dr.P.Selvam	Professor	ECE	hodeee@vmkvec.edu.in
2	Dr.T.Sheela	Associate Professor	ECE	sheela@vmkvec.edu.in

17ECCC81 - SEMICONDUCTOR DEVICES LAB

LIST OF EXPERIMENTS

1. Half Wave Rectifier
2. Full Wave Rectifier
3. Clipper
4. Clamper
5. Input/output Characteristics of CE Amplifier
6. Input/output Characteristics of CC Amplifier
7. Transfer Characteristics of JFET
8. Voltage Regulator
9. TRIAC, DIAC
10. SCR

Expt. No: 1

HALFWAVE RECTIFIERS WITH/WITHOUT FILTERS

AIM

Examine the input and output waveforms of a half wave rectifier without and with filters.Calculate the ripple factor with load resistance of 500Ω, 1 KΩ and 10 KΩ respectively.

Calculate ripple factor with a filter capacitor of 100□F and the load of 1K□, 2K□ and 10KΩ respectively.

COMPONENTS & EQUIPMENT REQUIRED

S.No	Device	Range/Rating	Quantity in No.
1	Rectifier and Filter trainer Board Containing a) AC Supply. b) Silicon Diodes c) Capacitor	 (9-0-9) V 1N 4007 0.47μF	 1 1 1
2	a) DC Voltmeter b) AC Voltmeter	(0-20) V (0-20) V	1 1
3	DC Ammeter	(0-50) mA	1
4	Cathode Ray Oscilloscope	(0-20) MHz	1
5	Decade Resistance Box	10Ω-100KΩ	1
6	Connecting wires	5A	12

THEORY

During positive half-cycle of the input voltage, the diode D1 is in forward bias and conducts through the load resistor R1. Hence the current produces an output voltage across the load resistor R1, which has the same shape as the +ve half cycle of the input voltage.

During the negative half-cycle of the input voltage, the diode is reverse biased and there is no current through the circuit. i.e, the voltage across R1 is zero. The net result is that only the +ve half cycle of the input voltage appears across the load. The average value of the half wave rectified o/p voltage is the value measured on dc voltmeter.

For practical circuits, transformer coupling is usually provided for two reasons.

1. The voltage can be stepped-up or stepped-down, as needed.
2. The ac source is electrically isolated from the rectifier. Thus preventing shock hazardsin the secondary circuit.

PROCEDURE

Half Wave Rectifier without filter

3. Connect the circuit as shown in figure (a).
4. Adjust the load resistance, R_L to 500Ω, and note down the readings of input and outputvoltages through oscilloscope.
5. Note the readings of dc current, dc voltage and ac voltage.
6. Now, change the resistance the load resistance, RL to 1 KΩ and repeat the procedure asabove. Also repeat for 10 KΩ.
7. Readings are tabulated as per the tabular column.

Half Wave Rectifier with filter

1. Connect the circuit as shown in figure (b) and repeat the procedure as for halfwave rectifier without filter.

CIRCUIT DIAGRAMS

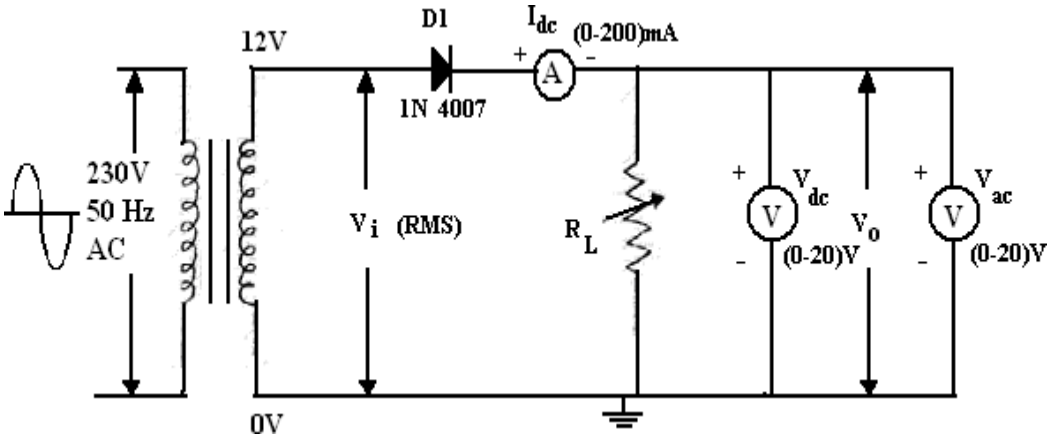


Figure (a) :Half Wave Rectifier without Filter

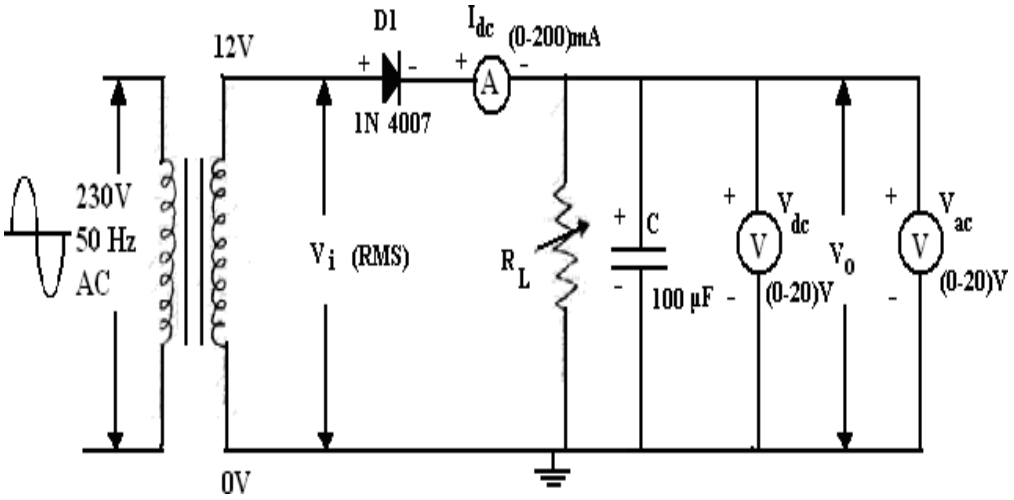
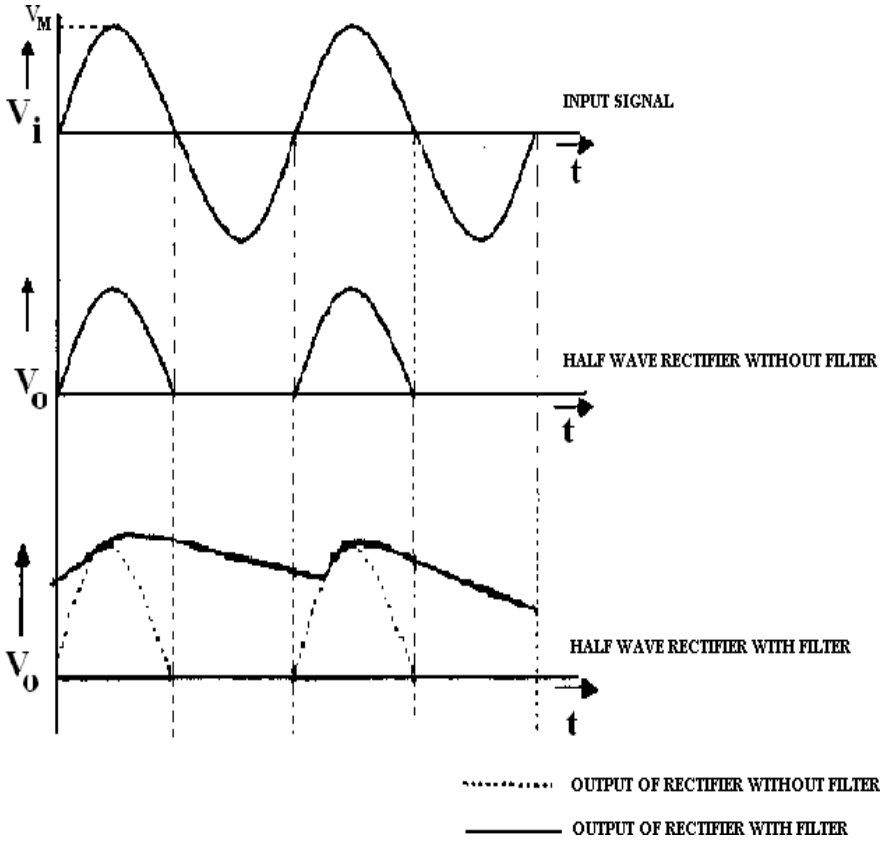


Figure (b):Half Wave Rectifier with Filter

EXPECTED GRAPHS



TABULAR COLUMNS

Half Wave Rectifier without Filter

S. No	**Load Resistance(R_L)**	**Input Voltage Peak (V_m)**	**Output Voltage Peak (V_o)**	**Average dc current (I_{dc})**	**Average Dc voltage(V_{dc})**	**RMS Voltage(V_{ac})**	**Ripple Factor** $\gamma = \frac{V_{ac}}{V_{dc}}$
1.	500Ω						
2.	1KΩ						
3.	10KΩ						

Half Wave Rectifier with Filter C=10μF

S. No	Load Resistance (R_L)	Input Voltage Peak (V_m)	Output Voltage Peak (V_o)	Averaged current (I_{dc})	AveageDc voltage (V_{dc})	RMS Voltage(V_{ac})	Ripple Factor$\gamma = \frac{V_{ac}}{V_{dc}}$
1.	1KΩ						
2.	2KΩ						
3.	10KΩ						

RESULT

Input and Output waveforms of a half-wave with /without filter are observed and plotted.

For Half-wave rectifier without filter-γ, Ripple factor at 500Ω=

1KΩ=

10 KΩ=

For Half-wave rectifier with filter:-γ, Ripple factor at 1KΩ, 100μF =

2KΩ, 100μF =

10 KΩ, 100μF =

Expt.No:2

FULLWAVE RECTIFIERS WITH/WITHOUT FILTER

AIM

Examine the input and output waveforms of a full wave (center tapped) rectifier without and withfilters.Calculate the ripple factor with load resistance of 500Ω, 1 KΩ and 10 KΩ respectively. Calculate ripple factor with a filter capacitor of 100□F and the load of 1K□, 2K□ and 10KΩ respectively.

COMPNENTS& EQUIPMENTS REQUIRED

S.No	Device	Range /Rating	Quantity (in No.s)
1	Rectifier and Filter trainer BoardContaining a) AC Supply. b) Silicon Diodes c) Capacitor	 (9-0-9) V 1N 4007 0.47μF	 1 2 1
2	a) DC Voltmeter b) AC Voltmeter	(0-20) V (0-20) V	1 1
3	DC Ammeter	(0-50) mA	1
4	Cathode Ray Oscilloscope	(0-20) MHz	1
5	Decade Resistance Box	10Ω-100KΩ	1
6	Electrolytic Capacitor	100μF	1
7	Connecting wires	5A	12

THEORY

The circuit of a center-tapped full wave rectifier uses two diodes D1&D2. During positive half cycle of secondary voltage (input voltage), the diode D1 is forward biased and D2is reverse biased.

The diode D1 conducts and current flows through load resistor R_L. During negative half cycle, diode D2 becomes forward biased and D1 reverse biased. Now, D2 conducts and current flowsthrough the load resistor R_L in the same direction. There is a continuous current flow through the load resistor R_L, during both the half cycles and will get unidirectional current as show in the model graph. The difference between full wave and half wave rectification is that a fullwave rectifier allows unidirectional (one way) current to the load during the entire 360 degreesof the input signal and half-wave rectifier allows this only during one half cycle (180 degree).

PROCEDURE

Full-wave Rectifier without filter

1. Connect the circuit as shown in the figure (a).
2. Adjust the load resistance R_L to 500Ω and connect a capacitor of 100μF value in parallelwith the load and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance RL to 2000Ω and repeat the procedure as the above.
5. Readings are tabulate as per the tabular column.

Full-wave Rectifier with filter

1. Connect the circuit as shown in the figure (b).
2. Adjust the load resistance R_L to 1KΩ and connect a capacitor of 100μF values in parallel with the load and note the readings of input and output voltages through Oscilloscope.
3. Note the readings of DC current, DC voltage and AC voltage.
4. Now change the load resistance R_L to 2KΩ and repeat the procedure as the above. Also
5. repeat for 10K, 100μF values.
6. Readings are tabulate as per the tabular column.

CIRCUIT DIAGRAMS

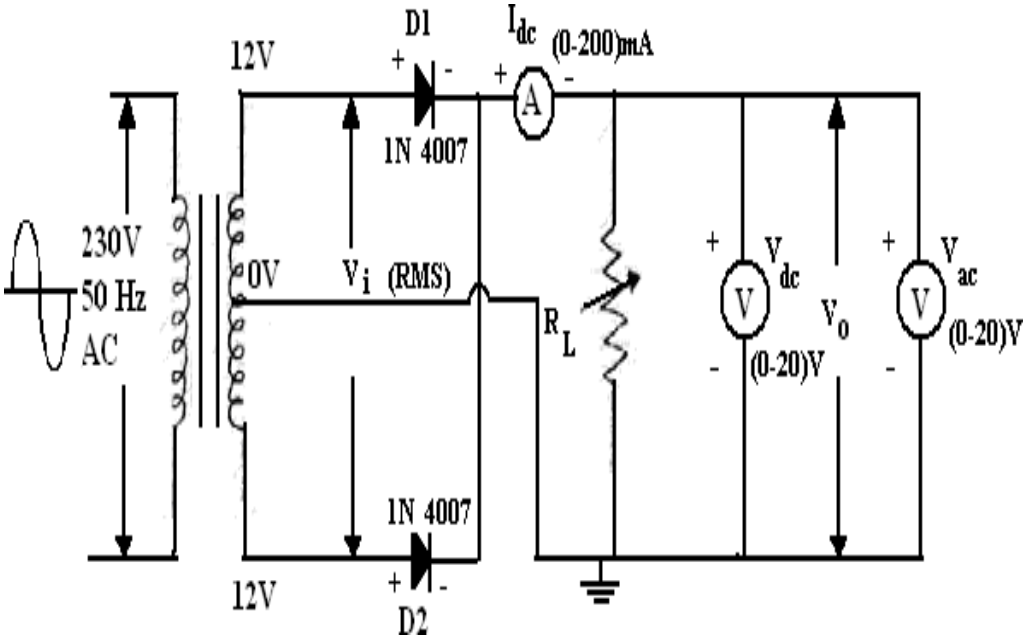


Figure (a): Full Wave Rectifier (Center-tap) Without Filter

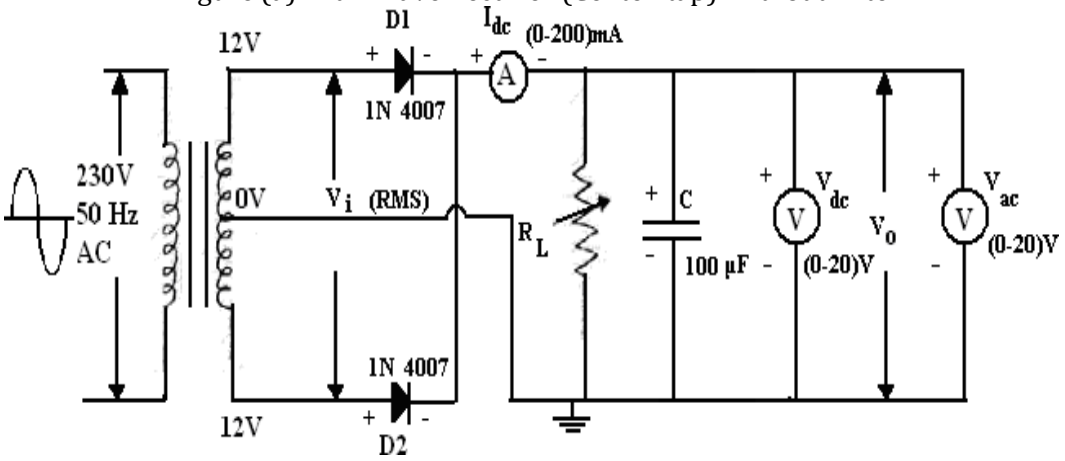
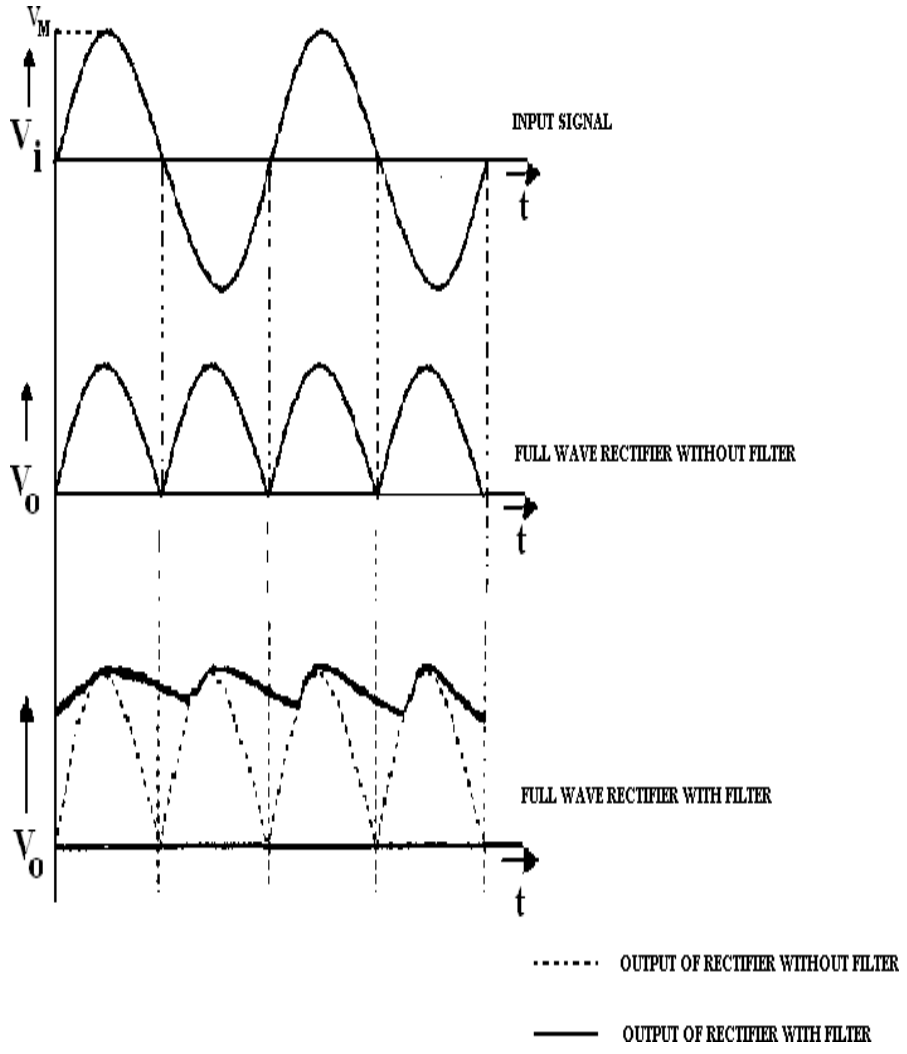


Figure (b): Full Wave Rectifier (center-tap) With Filter

EXPECTED GRAPHS



TABULAR COLUMNS

Full wave Rectifier (Center-tap) Without Filter

S. No	Load Resistance(R_L)	Input Voltage Peak (V_m)	Output Voltage Peak (V_o)	Average dc current (I_{dc})	AverageDc voltage (V_{dc})	RMS Voltage(V_{ac})	Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$
1	500Ω						
2	1KΩ						
3	10KΩ						

Full wave Rectifier (Center-tap) With Filter C = --- µF

S.No	Load Resistance(R_L)	Input Voltage Peak (V_m)	Output Voltage Peak (V_o)	Average dc current (I_{dc})	AverageDc voltage (V_{dc})	RMS Voltage(V_{ac})	Ripple Factor $\gamma = \frac{V_{ac}}{V_{dc}}$
1	500Ω						
2	1KΩ						
3	10K						

RESULT

Input and Output waveforms of a full-wave (center tapped) and bridge rectifier with /withoutfilters are observed and plotted.

For Full-wave rectifier(center tapped) without filter-

i. γ, Ripple factor at 500Ω, 100µF =

a. 2KΩ, 100µF =

For full-wave rectifier (Center tapped) with filter-

ii. γ, Ripple factor at 500Ω, 100µF =

Expt:No:3

Clipper Circuits

Aim:

To realize different clipping circuits and observe the waveforms.

Apparatus Required:

S.No	Item	Specification	Quantity
1	Step Down Transformer	220 V/12 V	1
2	Diode	IN4007	1
3	Resistor	1KΩ, 100 KΩ	1,1
4	Capacitor	1 micro Farad	1
5	RPS	(0-30) V	1
6	CRO		1
7	Connecting wires	------	------

THEORY

Clipping Circuits

Clipping circuits are nonlinear wave shaping circuits. A clipping circuit is useful to cutoff the positive or negative portions of an input waveform. Clipping circuits are also known as voltage limiters or slicers.

Positive clipper

The positive half cycle is clipped by diode and only the drop across diode will appear across the load. During negative half cycle, the diode does not conduct and the voltage across R_L is given by

$$V_L = V_S \frac{R_L}{R_L + R}$$

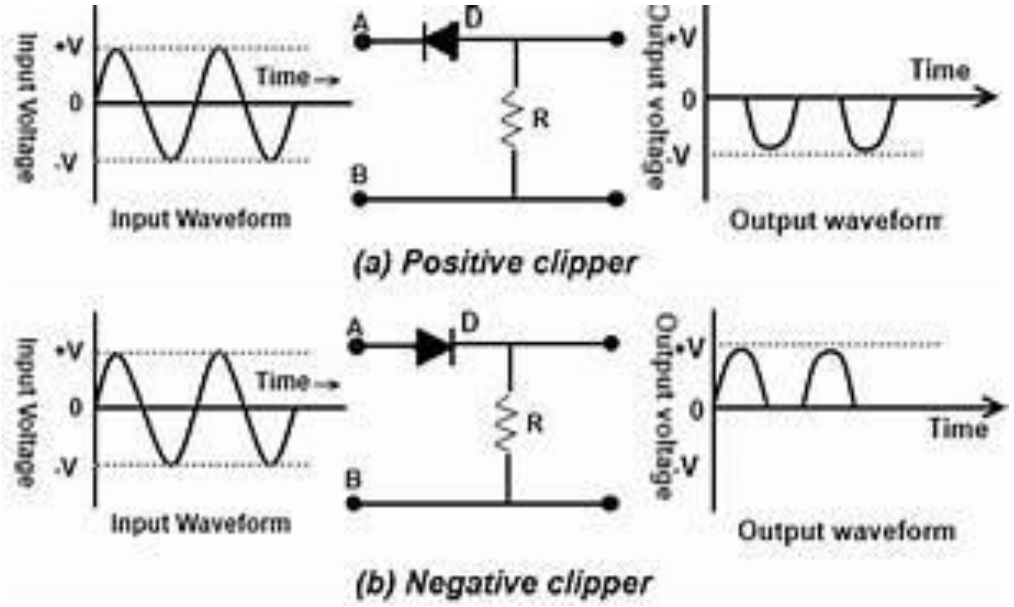
Since $R_L >> R$, the output voltage will be close to input voltage during negative half cycle.

Negative clipper

The negative half cycle is clipped by diode and only the drop across diode will appear across the load. During positive half cycle, the diode does not conduct and the voltage across R_L is given by

$$V_L = V_S \frac{R_L}{R_L + R}$$

Since R_L >> R, the output voltage will be close to input voltage during the positive half cycle



Procedure

1. The connections are made as per the circuit diagram.
2. Input AC Voltage is Given to the Circuit
3. The Output is viewed in CRO.
4. A graphs is drawn between Vm and t.

Result :

Thus the Clipper Circuits are verified and the Output is drawn in Graph.

Expt.No:4

Clampers Circuits

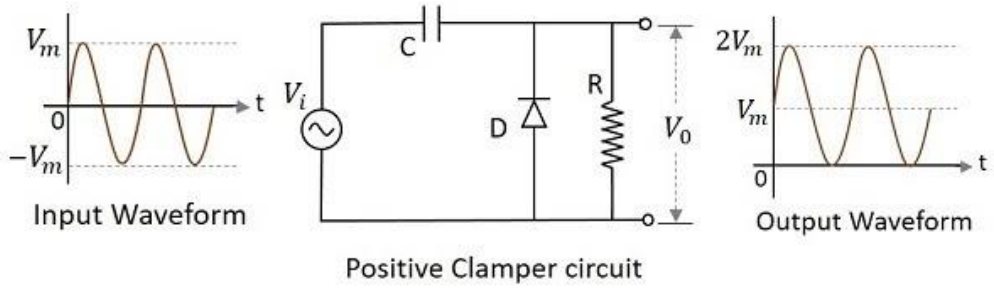
Aim:

To realize different clamping circuits and observe the waveforms.

Apparatus Required:

S.No	Item	Specification	Quantity
1	Step Down Transformer	220 V/12 V	1
2	Diode	IN4007	1
3	Resistor	1KΩ, 100 KΩ	1,1
4	Capacitor	1 micro Farad	1
5	RPS	(0-30) V	1
6	CRO		1
7	Connecting wires	------	------

THEORY



Procedure

1. The connections are made as per the circuit diagram.
2. Input AC Voltage is Given to the Circuit
3. The Output is viewed in CRO.
4. A graphs is drawn between Vm and t.

Result :

Thus the Clipper and Clamper Circuits are verified and the Output is drawn in Graph.

Expt.No:5

Input/output Characteristics of CE Amplifier

AIM

Plot the input and output characteristics of a transistor connected in CommonEmitter configuration.

COMPONENTS & EQUIPMENT REQUIRED

S.No	Device	Range /Rating	Quantity (in No.s)
1.	Transistor CE trainer BoardContaining a) DC Power Supply. b) PNP Transistor c) Carbon Film Resistor	 (0-12) V BC 107 470Ω, 1/2 W 100KΩ,1/2 W	 2 1 1 1
2.	a) DC Voltmeter b)DC Voltmeter	(0-1) V (0-20) V	1 1
3.	DC Ammeter	(0-50) mA (0-200) µA	1 1
4.	Connecting wires	5A	12

THEORY

A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitterconfiguration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals.

Therefore the emitter terminal is common to both input and output.

The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE}. Therefore input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between I_c and V_{CE} at constant I_B. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is

always constant and is approximately equal to I_B.

The current amplification factor of CE configuration is given by

$$B = \Delta I_C / \Delta I_B$$

PROCEDURE

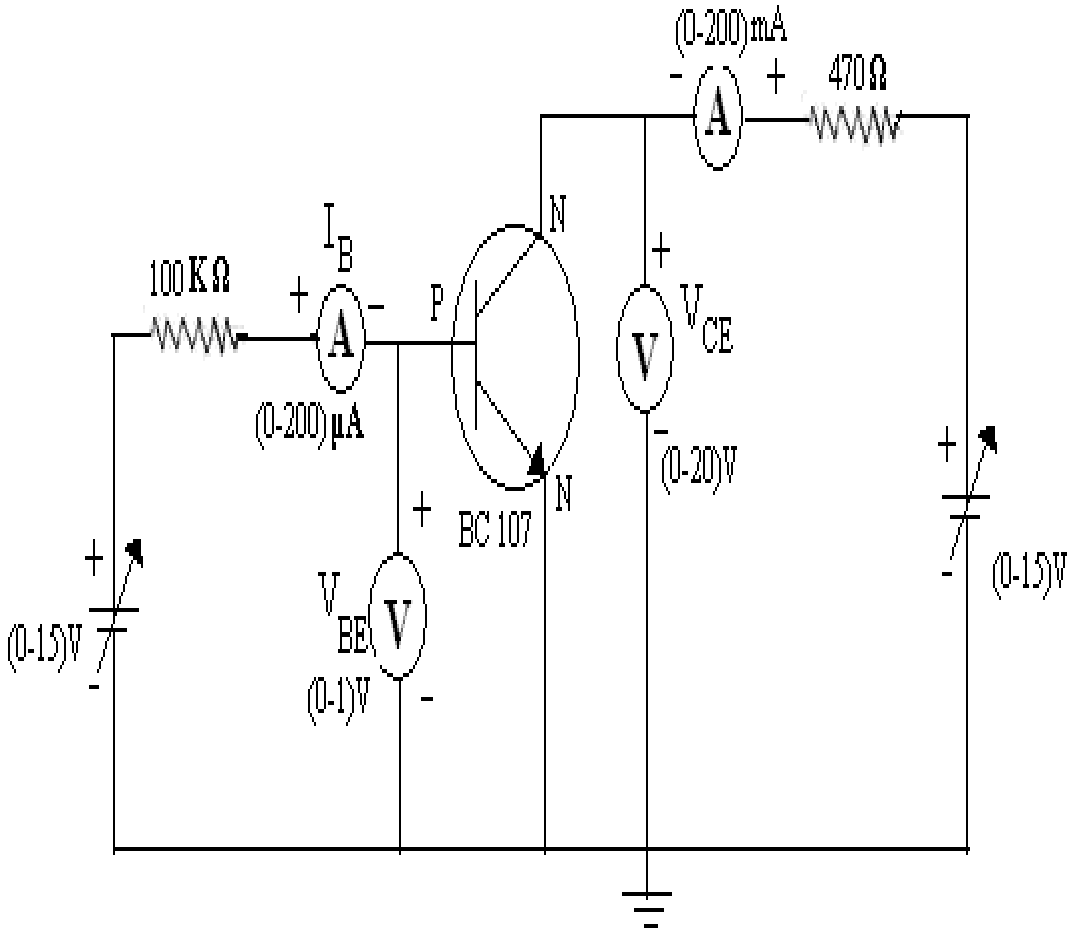
Input Characteristics:

1. Connect the transistor as shown in figure.
2. Keep the V_{CE} constant at 2V and 6V.
3. Vary the I_B in steps and note down the corresponding V_{EB} values as per tabular column.

Output Characteristics:

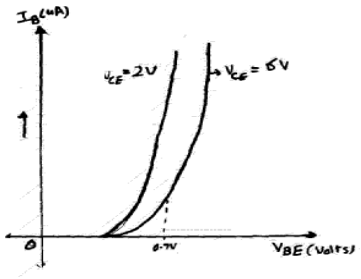
1. Keep the I_B constant at 20 μA and 40 μA.
2. Vary the V_{CE} in steps and note corresponding I_C values.
3. Readings are tabulated as shown in tabular column.

CIRCUIT DIAGRAM

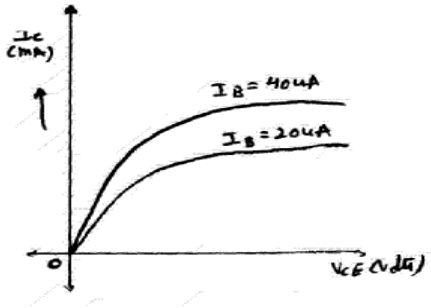


EXPECTED GRAPHS

Input Characteristics



Output Characteristics



TABULAR COLUMN

Input Characteristics

V_{CB} = 2V		V_{CB} = 6V	
V_{BE} (Volts)	I_B (µA)	V_{BE} (Volts)	I_B (µA)

Output Characteristics

I_B = 20µA		I_B = 40µA	
V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)

RESULT

Input and Output curves are plotted.

Expt.No:6

Input/output Characteristics of CC Amplifier

AIM

Plot the input and output characteristics of a transistor connected in CommonCollector configuration.

COMPONENTS & EQUIPMENT REQUIRED

S.No	Device	Range /Rating	Quantity (in No.s)
1.	Transistor CC trainer BoardContaining d) DC Power Supply. e) PNP Transistor f) Carbon Film Resistor	 (0-12) V BC 107 470Ω, 1/2 W 100KΩ,1/2 W	 2 1 1 1
2.	c) DC Voltmeter d)DC Voltmeter	(0-1) V (0-20) V	1 1
3.	DC Ammeter	(0-50) mA (0-200) μA	1 1
4.	Connecting wires	5A	12

Input Characteristics:

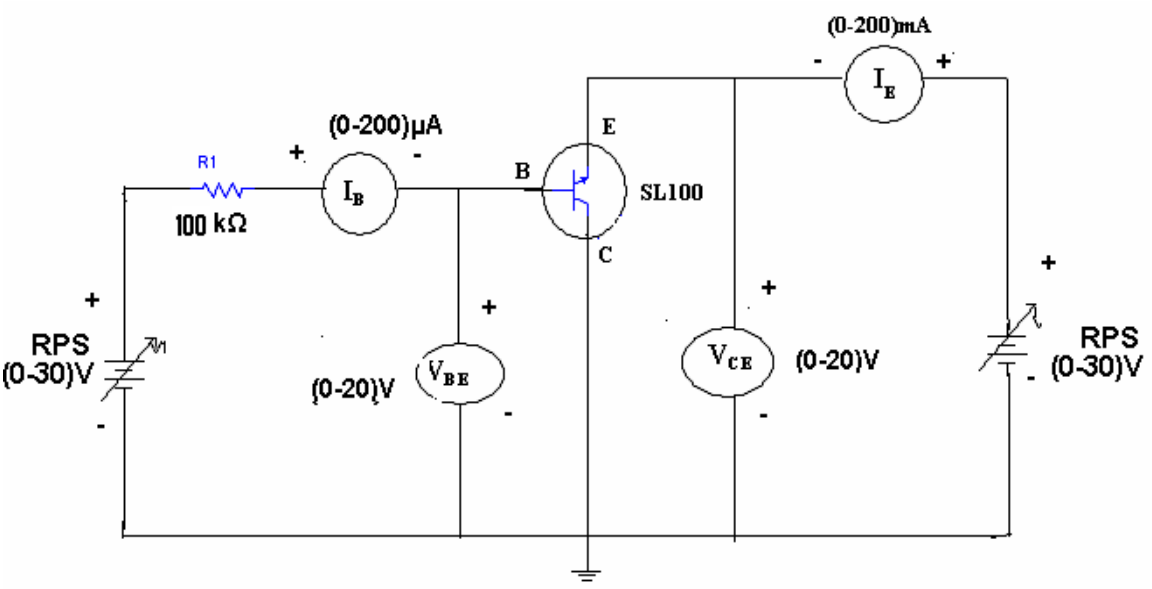
1. Connect the transistor as shown in figure.
2. Keep the V_{CE} constant at 2V and 6V.
3. Vary the I_B in steps and note down the corresponding V_{EB} values as per tabular column.

Output Characteristics:

a. Keep the I_B constant at 20 μA and 40 μA.

b. Vary the V_{CE} in steps and note corresponding I_C values.

c. Readings are tabulated as shown in tabular column.



TABULAR COLUMN

Input Characteristics

V_{CB} = 2V		V_{CB} = 6V	
V_{BE} (Volts)	I_B (μA)	V_{BE} (Volts)	I_B (μA)

Output Characteristics

I_B = 20μA		I_B = 40μA	
V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)

RESULT

Input and Output curves are plotted.

Expt.No:7

Transfer Characteristics of JFET

AIM: To Draw the Characteristics Curves of JFET

COMPONENTS & EQUIPMENTS REQUIRED:

S.No.	Device	Range /Rating	Quantity (In No.s)
1	FET Characteristics trainer board containing		
	(a) DC power supply	0-12V	1
	(b) DC power supply	0-5V	1
	(c) FET	BFW 11	1
	(d) Carbon film resistor	1K, 1/2W	1
	(e) Carbon film resistor	470K, 1/2W	1
2	DC Voltmeter	0-20V	2
3	(a) DC Ammeter	0-200A	1
	(b) DC Ammeter	0-20mA	1
4	Connecting wires		12

THEORY:

A FET is a three terminal device, having the characteristics of high input impedance and less noise, the Gate to Source junction of the FET s always reverse biased. In response to small applied voltage from drain to source, the n-type bar acts as sample resistor, and the drain current increases linearly with $V_{DS.}$ With increase in I_D the ohmic voltage drop between the source and the channel region reverse biases the junction and the conducting position of the channel begins to remain constant. The V_{DS} at this instant is called “pinch of voltage”.

If the gate to source voltage (V_{GS}) is applied in the direction to provide additional reverse bias, the pinch off voltage ill is decreased.

In amplifier application, the FET is always used in the region beyond the pinch-off.

$$F_{DS}=I_{DSS}(1-V_{GS}/V_P)^2$$

PROCEDURE: -

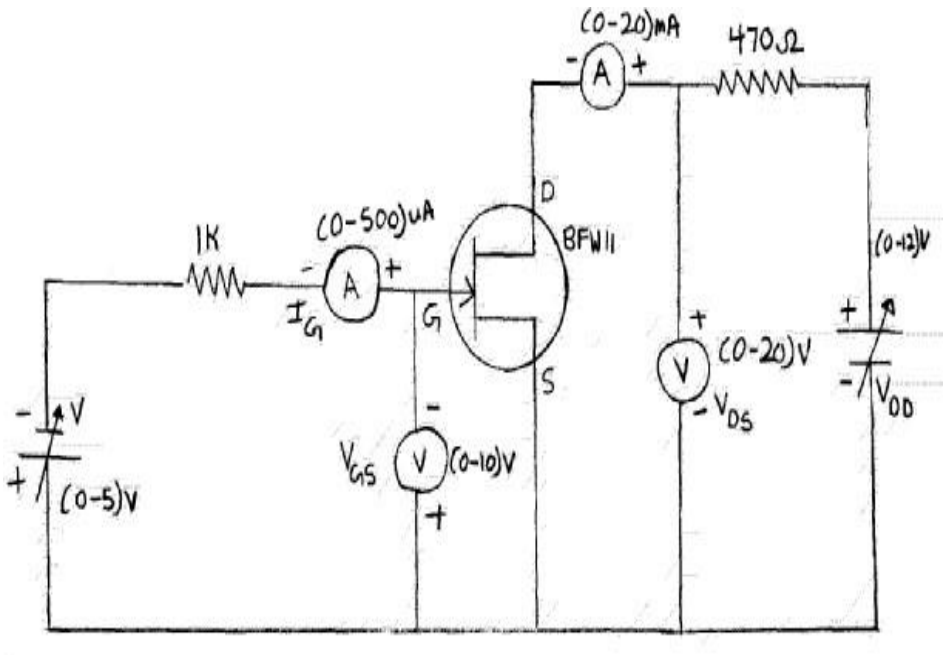
Drain characteristics:

1. Connect the circuit as shown in figure (1)
2. Set the gate source voltage, V_{GS} in 0V position.
3. Increase drain source voltage, V_{DS} in steps and note corresponding I_D values asShown in the tabular column.
4. Now change V_{GS} to +0.5Vand –1V and repeat the above procedure.

Transfer characteristics:

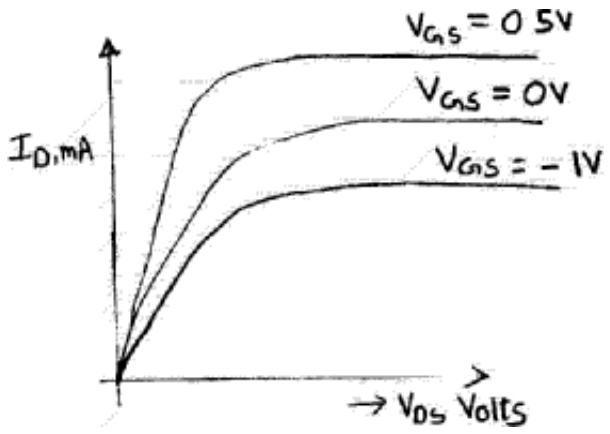
5. Connect the circuit as shown in figure (1).
6. Keep the drain source voltage, V_{DS} at 1V.
7. Vary the gate source voltage, V_{GS} in steps and note corresponding I_D values as shownin the tabular column.
8. Now change V_{DS} to 2Vand 3V and repeat the above procedure.

CIRCUIT DIAGRAM:

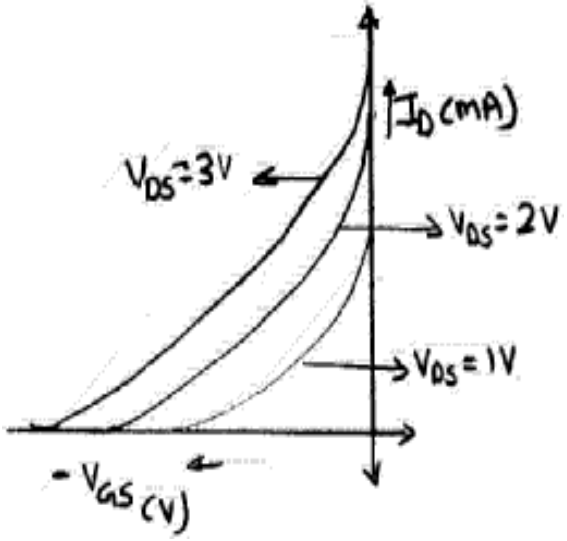


EXPECTED GRAPHS:

Drain Characteristics:



Transfer Characteristics:



TABULATIONS:

Drain characteristics:

	V_{GS}=0V	V_{GS}= 0.5V	V_{GS}= 1.0V
V_{DS} (v)	I_D (mA)	I_D (mA)	I_D (mA)
0			
0.2			
0.4			
0.6			
0.8			
1.0			
2.0			
3.0			
4.0			
5.0			
6.0			
7.0			
8.0			
9.0			
10.0			

Transfer characteristics:

	V_{DS}=0V	V_{DS}=2V	V_{DS}= 3V
V_{GS} (v)	I_D (mA)	I_D (mA)	I_D (mA)
0			
-0.2			
-0.4			
-0.6			
-0.8			
-1.0			
-1.2			
-1.4			

-1.6			
-1.8			
-2.0			
-2.2			
-2.4			
-2.6			
-2.8			

CALCULATIONS:

a. AC drain resistance at V_{DS}=3V of V_{GS}= 0.5V
   i. = $\Delta V_{DS} / \Delta I_D$
   ii. =
b. AC drain resistance at V_{DS}=3V of V_{GS}= 0V
   i. = $\Delta V_{DS} / \Delta I_D$
   ii. =
c. AC drain resistance at V_{DS}=3V of V_{GS}= -1V
   i. = $\Delta V_{DS} / \Delta I_D$
   ii. =
d. Transconductance at V_{GS} = -1V of V_{DS}=1V
   i. = $\Delta I_D / \Delta V_{GS}$
   ii. =
e. Transconductance at V_{GS} = -1V of V_{DS}=2V
   i. = $\Delta I_D / \Delta V_{GS}$
f. Transconductance at V_{GS} = -1V of V_{DS}=3V
   i. = $\Delta I_D / \Delta V_{GS}$

RESULT:

Thus the Drain and Transfer Characteristics of JFET was Drawn.

Expt. No:8

Voltage Regulator

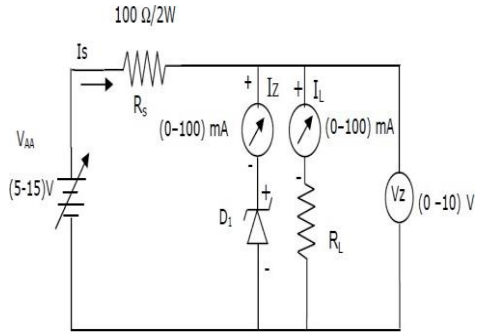
Aim:

To study zener diode as voltage regulator

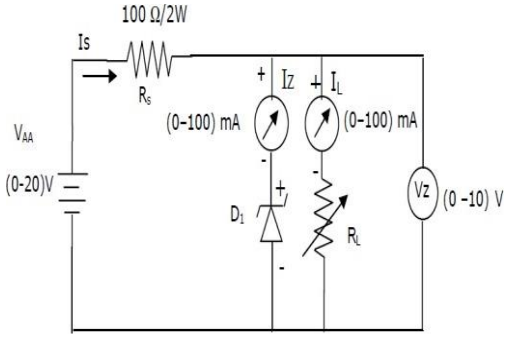
Apparatus Required:

S.No	Item	Specification	Quantity
1	Step Down Transformer	220 V/12 V	1
2	Zener Diode	IN4007	1
3	Resistor	1KΩ, 100 KΩ	1,1
4	Voltmeter	0-10 V	1
5	Ammeter	0-100mA)	2
6	RPS	(0-30) V	1
7	CRO		1
8	Connecting wires	------	------

CIRCUIT DIAGRAM:



Line Regulation: Zener Regulator



Load Regulation: Zener Regulator

THEORY:

Zener diode is a P-N junction diode specially designed to operate in the reverse biased mode. Itis acting as normal diode while forward biasing. It has a particular voltage known as break down voltage, at which the diode break downs while reverse biased. In the case of normal diodes the diode damages at the break down voltage. But Zener diode is specially designed to operate in thereverse breakdown region.

The basic principle of Zener diode is the Zener breakdown. When a diode is heavily doped, it's depletion region will be narrow. When a high reverse voltage is applied across the junction, therewill be very strong electric field at the junction. And the electron hole pair generation takesplace. Thus heavy current flows. This is known as Zener break down.

So a Zener diode, in a forward biased condition acts as a normal diode. In reverse biased mode, after the break down of junction current through diode increases sharply. But the voltage acrossit remains constant. This principle is used in voltage regulator using Zener diodes

The figure shows the zener voltage regulator, it consists of a current limiting resistor RS connected in series with the input voltage Vs and zener diode is connected in parallel with the load RL in reverse biased condition. The output voltage is always selected with a breakdown voltage Vz of the diode.

e input source current, IS = IZ + IL..... (1)

The drop across the series resistance, Rs = Vin – Vz .....(2)

And current flowing through it, Is = (Vin – VZ) / RS.....(3)

From equation (1) and (2), we get, (Vin - Vz)/Rs = Iz +IL..... (4)

Regulation with a varying input voltage (line regulation): It is defined as the change in regulated voltage with respect to variation in line voltage. It is denoted by 'LR'.

In this, input voltage varies but load resistance remains constant hence, the load current remains constant. As the input voltage increases, form equation (3) Is also varies accordingly. Therefore, zener current Iz will increase. The extra voltage is dropped across the Rs. Since, increased Iz willstill have a constant Vz and Vz is equal to Vout.

The output voltage will remain constant. If there is decrease in Vin, Iz decreases as load current remains constant and voltage drop across Rs is reduced. But even though Iz may change, Vz remains constant hence, output voltage remains constant.

Regulation with the varying load (load regulation): It is defined as change in load voltage with respect to variations in load current. To calculate this regulation, input voltage is constant and output voltage varies due to change in the load resistance value.

Consider output voltage is increased due to increasing in the load current. The left side of the equation (4) is constant as input voltage Vin, IS and Rs is constant. Then as load current changes,the zener current Iz will also change but in opposite way such that the sum of Iz and IL will remain constant. Thus, the load current increases, the zener current decreases and sum remain constant. Form reverse bias characteristics even Iz changes, Vz remains same hence, and output voltage remains fairly constant.

PROCEDURE:-

Line Regulation:

1. Make the connections as shown in figure below.
2. Keep load resistance fixed value; vary DC input voltage from 5V to 15V.

3. Note down output voltage as a load voltage with high line voltage 'VHL' and as a loadvoltage with low line voltage 'VLL'.
4. Using formula, % Line Regulation = (VHL-VLL)/ VNOM x100, where VNOM = the nominal load voltage under the typical operating conditions. For ex. VNOM = 9.5 ± 4.5 V

Load Regulation:

1. For finding load regulation, make connections as shown in figure below.
2. Keep input voltage constant say 10V, vary load resistance value.

3. Note down no load voltage 'VNL' for maximum load resistance value and full load voltage'VFL' for minimum load resistance value.
4. Calculate load regulation using, % load regulation = (VNL-VFL)/ VFL x100

OBSERVATION TABLE:-

Zener Voltage	Load Current

Result:

Thus the Zener Voltage Regulator was designed

Expt.No:9

SCR Characteristics

Aim: -

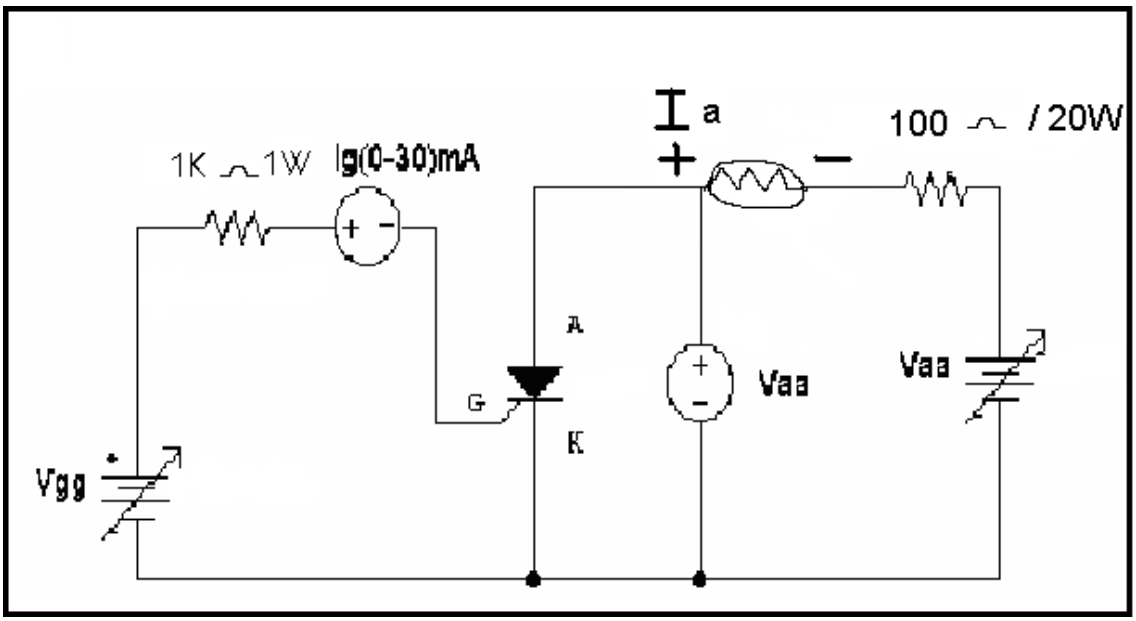
To study the V-I characteristics of S.C.R. and determine the Break overvoltage, on state resistance Holding current. & Latching current

Apparatus required: -

SCR – TY604, Power Supplies, Wattage Resistors, Ammeter, Voltmeter, etc.,

Procedure: -

1. Connections are made as shown in the circuit diagram.
2. The value of gate current I_G, is set to convenient value by adjusting V_{GG}.
3. By varying the anode- cathode supply voltage V_{AA} gradually in step-by-step, note down the corresponding values of V_{AK} & I_A. Note down V_{AK} & I_A at the instant of firing of SCR and after firing (by reducing the voltmeter ranges and in creasing the ammeter ranges) then increase the supply voltage V_{AA}. Note down corresponding values of V_{AK} & I_A.
4. The point at which SCR fires, gives the value of break over voltage V_{BO}.
5. A graph of V_{AK} V/S I_A is to be plotted.
6. The on state resistance can be calculated from the graph by using a formula.
7. The gate supply voltage V_{GG} is to be switched off
8. Observe the ammeter reading by reducing the anode-cathode supply voltage V_{AA}. The point at which the ammeter reading suddenly goes to zero gives the value of Holding Current I_H.
9. Steps No.2, 3, 4, 5, 6, 7, 8 are repeated for another value of the gate current I_G.



Tabular column: -

I_g = mA I_g =

Sl.No	V_{AK} Volts	I_A µA/mA/A

Sl.No	V_{AK} Volts	I_A µA/mA/A

Procedure (Latching current)

1. connections one made as shown in the circuit diagram
2. Set Vgg at 7 volts
3. Set V_{aa} at particular value, observe I_a, by operating the switch (on & off).if in goes to zero after opening of the switch, indicates $I_a < I_L$
4. Repeat step 3 such that the current I_a should not go to zero after openingof the switch. Then I_a gives the value of I_L.

Result:
Thus the Characteristics Curve of SCR is Drawn.

Expt.No10:

TRIAC Characteristics

Aim: -

To study the v-1 characteristics of a TRIAC in both directions and also in different (1, 2, 3 & 4) modes op operation and determine break over voltages, holding current, latching current and comment on sensitivities.

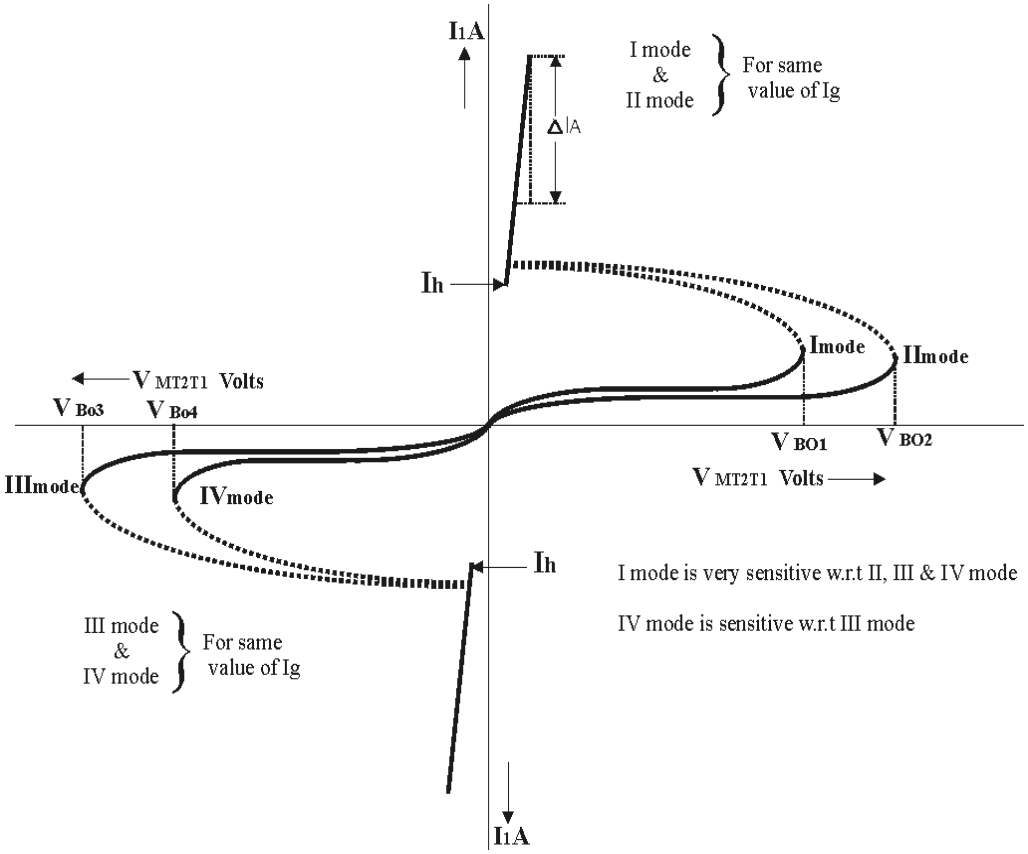
Apparatus required: -

TRIAC – BT 136, power supplies, wattage resistors, ammeter, voltmeter, etc.,

Proce

dure: -

1. Connections are made as shown in the circuit diagram (a)
2. The value of gate current i_g is set to convenient value by adjusting v_{gg}.
3. By varying the supply voltage V_m gradually in step-by-step, note down thecorresponding values of V_{mt2t1} and i_1. Note down V_{mt2t1} and i_1 at the instantof firing of TRIAC and after firing (by reducing the voltmeter ranges and increasing the ammeter ranges) then increase the supply voltage V_{mt2mt1} and i_1.
4. The point at which TRIAC fires gives the value of break over voltage v_{bo1}
5. A graph of v_{mt2t1} v/s i_1 is to be plotted.
6. The gates supply voltage. V_{gg} is to be switched off
7. Observe the am meter reading by reducing the supply voltage v_{mt}. The point at which the ammeter reading suddenly goes to zero gives the valueof holding current $i_{h.}$



I-mode

Tabular Coloumn:

i g = ma

Sl.no	V_{TRIAC} volts	I_{TRIAC} ma

Result:

Thus The TRIAC Characteristics Curve was Drawn.