PROG, BRANCH,	**B. E., E. C. E**
YEAR, SEMESTER, SECTION	**II / III, -**
SUBJECT	**17ECCC82 - DIGITAL LOGIC CIRCUITS & DESIGN LAB**
ACADEMIC YEAR	**2021-2022 (ODD SEMESTER)**

LIST OF EXPERIMENTS:

Hardware Experiments

1. Design and implementation of Adders using logic gates.
2. Design and implementation of Sub tractors using logic gates.
3. Design and implementation of BCD to Excess -3 code converter using logic gates
4. Design and implementation of Binary to Gray code converter using logic gates
5. Design and implementation of 4 bit BCD adder using IC 7483
6. Design and implementation of 2 Bit Magnitude comparator using logic gates
7. Design and implementation of Multiplexer and De-Multiplexer using logic gates
8. Design and implementation of encoder and decoder using logic gates
9. Design and implementation of 3 bit synchronous up/down counter.
10. Implementation of SISO, SIPO, and PISO shift registers using flip flops.

Software Experiments using HDL

1. Design and Simulation of Full adder circuit using Gate level modelling
2. Design and Simulation of 2X2 multiplier circuit using structural level modeling.
3. Design and Simulation of 8 to 1 Multiplexer circuit using behavioural level modeling.

HOD / ECE